DATASHEET
ADDENDUM

Intel 82371AB PCI ISA IDE Xcelerator (PIIX4)

Timing Specification

273135-001

October, 1997

82371AB PCI ISA IDE Xcelerator (PIIX4) Features

- **Supported Kits for both Pentium® and Pentium® Pro Microprocessors**
  - — 82430TX ISA Kit
  - — 82440LX ISA/DP Kit
- **Multifunction PCI to ISA Bridge**
  - — Supports PCI at 30 MHz and 33 MHz
  - — Supports PCI Rev 2.1 Specification
  - — Supports Full ISA or Extended I/O (EIO) Bus
  - — Supports Full Positive Decode or Subtractive Decode of PCI
  - — Supports ISA/EIO at 1/4 of PCI Frequency
- **Supports Both Mobile and Desktop Deep Green Environments**
  - — 3.3 V Operation With 5 V Tolerant Buffers
  - — Ultra-Low Power for Mobile Environments
  - — Power-On Suspend and Soft-OFF for Desktop Environment
  - — All Registers Readable/Restorable for Proper Resume From 0 V Suspend
- **Power Management Logic**
  - — Global and Local Device Management
  - — Suspend/Resume Logic
  - — Supports Thermal Alarm
  - — Support for External Microcontroller
  - — Full Support for Advanced Configuration and Power Interface (ACPI) Specification and OS Directed Power Management
- **Enhanced DMA Controller**
  - — Two 82C37 DMA Controllers
  - — Supports PCI DMA With 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - — Fast Type-F DMA for Reduced PCI Bus Usage
- **Integrated IDE Controller**
  - — Independent Timing of Up to 4 Drives
  - — PIO Mode 4 Transfers Up to 14 Mbytes/s
  - — Supports “Ultra DMA/33” Synchronous DMA Mode Transfers Up to 33 Mbytes/s
  - — Integrated 8 x 32-Bit Buffer for IDE PCI Burst Transfers
  - — Supports Glue-Less “Swap-Bay” Option With Full Electrical Isolation
- **Interrupt Controller Based on Two 82C59**
  - — 15 interrupt support
  - — Independently Programmable for Edge/Level Sensitivity
  - — Supports Optional I/O APIC
  - — Serial Interrupt Input
- **Timers based on 82C54**
  - — System Timer, Refresh Request, Speaker Tone Output
- **USB**
  - — Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/s
  - — Supports Legacy Keyboard and Mouse Software With USB-Based Keyboard and Mouse
  - — Supports UHCI Design Guide Revision 1.1 Interface
- **SMBus**
  - — Host interface Allows CPU to Communicate via SMBus
  - — Slave Interface Allows External SMBus Master to Control Resume Events
- **Real-Time Clock**
  - — 256-Byte Battery-Back CMOS SRAM
  - — Includes Date Alarm
  - — Two 8-Byte Lockout Ranges
- **Microsoft* Windows 95* Compliant**
- **324 mBGA Package**

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 82371AB (PIIX4) PCI ISA IDE Xcelerator. Please refer to the standard package datasheet (order number 290562 for the PIIX4) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

The 82371AB (PIIX4) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel retains the right to make changes to specifications and product descriptions at any time, without notice.

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Intel 82371AB PCI ISA IDE Xcelerator (PIIX4) Timing Specification

FIGURES

TABLES

1.0 Introduction

This document contains the electrical and the thermal specifications for the 82371AB (PIIX4). PIIX4 is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus Host/Hub function, and a Power Management function.

The contents of this document are based on simulation and parametric data. This information may be modified as more data is available.

1.1 References

The reader should be familiar with the following documents:

- *82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet
- Universal Serial Bus Specification
- *Universal Host Controller Interface (UHCI) Design Guide*
- System Management Bus Specification
- Serialized IRQ Support for PCI Systems Specification
- Distributed DMA Support for PCI Systems Specification

2.0 Electrical Characteristics

2.1 Absolute Maximum Ratings

Case temperature under bias .... 0° C to +85° C
Storage temperature .... -55° C to +150° C
Voltage on any pin with respect to ground .... -0.3 to V_{CC} +0.3 V
3.3 V supply voltage with respect to V_{SS} .... -0.3 to +4.6 V
5.0 V supply voltage with respect to V_{SS} (VREF) .... -0.3 to +5.5 V
Maximum Power Dissipation .... 1.0 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

The 82371AB PIIX4 (BGA) is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the package are given in Table 1.

Table 1. Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	**1.0 (196.9)**
θ_{ja} (°C/Watt)	29	24.5
θ_{jc} (°C/Watt)	9.0	

2.2 D.C. Characteristics

Table 2. DC Characteristics (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}(RTC)	Battery Voltage	2.0	3.6	V	
V_{CC}(SUS)	Standby Voltage	3.0	3.6	V	
V_{IL1}	Input Low Voltage	-0.5	0.3 V_{CC}	V	1
V_{IH1}	Input High Voltage	0.5 V_{CC}	V_{CC} + 0.5	V	1
V_{IL2}	Input Low Voltage	-0.3	0.6	V	1
V_{IH2}	Input High Voltage	1.4	V_{CC} + 0.3	V	1
V_{IL3}	Input Low Voltage	-0.5	0.8	V	1
V_{IH3}	Input High Voltage	2.0	VCC5 + 0.5	V	1
V_{OL1}	Output Low Voltage		0.4	V	1
V_{OH1}	Output High Voltage	V_{CC} - 0.5		V	1
V_{OL2}	Output Low Voltage		0.3	V	1, 2
V_{OH2}	Output High Voltage	2.8	3.6	V	1, 2
V_{OL3}	Output Low Voltage		0.5	V	1
V_{OH3}	Output High Voltage	V_{CC} - 0.5		V	1
V_{OL4}	Output Low Voltage		0.45	V	1
V_{OH4}	Output High Voltage	V_{CC} - 0.5		V	1
V_{DI}	Differential Input Sensitivity	0.2		V	|(USBPx+, USBPx-)|
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Includes V_{DI}
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	
I_{OL1}	Output Low Current		4	mA	1, @ V_{OL1}
I_{OH1}	Output High Current	-1		mA	1, @ V_{OH1}
I_{OL2}	Output Low Current		10	mA	1, @ V_{OL4}
I_{OH2}	Output High Current	-3		mA	1, @ V_{OH4}
I_{OL3}	Output Low Current		3	mA	1, @ V_{OL1}
I_{OH3}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL4}	Output Low Current		6	mA	1, @ V_{OL1}
I_{OH4}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL5}	Output Low Current		2	mA	1, @ V_{OL2}

NOTES:

1. Refer to Table 3 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 KΩ to 3.6 V and V_{OH2} assumes R_L of 15 KΩ to GND.

Table 2. DC Characteristics (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
I_{OH5}	Output High Current	-0.25		mA	1, @ V_{OH2}
I_{OL6}	Output Low Current		6	mA	1, @ V_{OL1}
I_{OH6}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL7}	Output Low Current		7	mA	1, @ V_{OL1}
I_{OH7}	Output High Current	-2		mA	1, @ V_{OH1}
I_{OL8}	Output Low Current		11	mA	1, @ V_{OL3}
I_{OH8}	Output High Current	-2		mA	1, @ V_{OH3}
I_{LI1}	Input Leakage Current		± 1	µA	
I_{LI2}	Hi-Z State Data Line Leakage	-10	+10	µA	(0 V< V_{IN}< 3.3 V)
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz
C_L	Crystal Load Capacitance	7.5	15	pF	

NOTES:

1. Refer to Table 3 for the signals associated with this specification.
2. V_{OL2} assumes R_L of 1.5 KΩ to 3.6 V and V_{OH2} assumes R_L of 15 KΩ to GND.

Table 3. DC Characteristic Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
V_{IL1} / V_{IH1}	**V_{REF}=5.0 V:** (all 3.3 V only inputs except SMBCLK & SMBDATA) PWROK, RSMRST#, RTCX1, TEST, BATLOW#, CONFIG[1:2], EXTSMI#, GPI[1], IRQ8#, LID, RI#, SMBALERT#, PWRBTN#, USBP[1:0]+, USBP[1:0]-, FERR# **V_{REF}=3.3 V:** (all inputs except SMBCLK & SMBDATA) PWROK, RSMRST#, RTCX1, TEST, BATLOW#, CONFIG[1:2], EXTSMI#, GPI[1], IRQ8#, LID, RI#, SMBALERT#, PWRBTN#, USBP[1:0]+, USBP[1:0]-, FERR#, AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IDSEL, IRDY#, PHLDA#, SERR#, STOP#, TRDY#, IOCHK#, IOCHRDY, IOCS16#, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, SA[19:0], SBHE#, SD[15:0], ZEROWS#, A20GATE, RCIN#, DREQ[0:3, 5:7], REQ[A:C]#, APICREQ#, IRQ[1, 3:7, 9:12, 14:15], PIRQ[A:D], SERIRQ, CLK48, PCICLK, OSC, PDD[15:0], PDDREQ, PIORDY, SDD[15:0], SDDREQ, SIORDY, OC[1:0]#, PCIREQ[A:D],THRM#
V_{IL2} / V_{IH2}	SMBCLK, SMBDATA
V_{IL3} / V_{IH3}	**V_{REF}=5.0 V:** (all 5 V tolerant inputs) AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IDSEL, IRDY#, PHLDA#, SERR#, STOP#, TRDY#, IOCHK#, IOCHRDY, IOCS16#, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, SA[19:0], SBHE#, SD[15:0], ZEROWS#, A20GATE, RCIN#, DREQ[0:3, 5:7], REQ[A:C]#, APICREQ#, IRQ[1, 3:7, 9:12, 14:15], PIRQ[A:D], SERIRQ, CLK48, PCICLK, OSC, PDD[15:0], PDDREQ, PIORDY, SDD[15:0], SDDREQ, SIORDY, OC[1:0]#, PCIREQ[A:D],THRM#
V_{OL1} / V_{OH1}	PDA[2:0], PDCS1#, PDCS3#, PDD[15:0], PDDACK#, PDIOR#, PDIOW#, SDA[2:0], SDCS1#, SDCS3#, SDD[15:0], SDDACK#, SDIOR#, SDIOW#, CPU_STP#, EXTSMI#, ZZ, GPO8, PCI_STP#, SMBCLK, SMBDATA, SUS[A:C]#, SUS_STAT[1:2]#, A20M#, CPURST, IGNNE#, INIT, INTR, NMI, SMI#, STPCLK#, BIOSCS#, KBCCS#, MCCS#, PCS0#, PCS1#, RTCALE, RTCCS#, XDIR#, XOE#, SUSCLK, RTCX2, SMBCLK, SMBDATA, APICACK#, APICCS#, IRQ[0, 8], SPKR, GNT[A:C], GPO[0, 8, 27, 28, 30], IRQ9OUT#, AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IRDY#, PAR, PCIRST#, PHOLD#, SERR#, STOP#, TRDY#, SERIRQ
V_{OL2} / V_{OH2}	USBP[1:0]+, USBP[1:0]-
V_{OL3} / V_{OH3}	SLP#
V_{OL4} / V_{OH4}	**ISA/EIO Output Signals:** AEN, BALE, IOCHRDY, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, RSTDRV, SA[19:0], SBHE#, SD[15:0], SMEMR#, SMEMW#, SYSCLK, DACK[0:3, 5:7]#, TC
I_{OL1} / I_{OH1}	**IDE Output Signals:** PDA[2:0], PDCS1#, PDCS3#, PDD[15:0], PDDACK#, PDIOR#, PDIOW#, SDA[2:0], SDCS1#, SDCS3#, SDD[15:0], SDDACK#, SDIOR#, SDIOW#
I_{OL2} / I_{OH2}	**ISA/EIO Output Signals:** AEN, BALE, IOCHRDY, IOR#, IOW#, LA[23:17], MEMCS16#, MEMR#, MEMW#, REFRESH#, RSTDRV, SA[19:0], SBHE#, SD[15:0], SMEMR#, SMEMW#, SYSCLK, DACK[0:3, 5:7]#, TC

Table 3. DC Characteristic Signal Association (Sheet 2 of 2)

Symbol	Associated Signals
I_{OL3} / I_{OH3}	**Power Management Signals:** CPU_STP#, EXTSMI#, ZZ, GPO8, PCI_STP#, SMBCLK, SMBDATA, SUS[A:C]#, SUS_STAT[1:2]# **CPU Interface Signals:** A20M#, CPURST, IGNNE#, INTR, NMI **X-Bus Interface Signals:** BIOSCS#, KBCCS#, MCCS#, PCS0#, PCS1#, RTCALE, RTCCS#, XDIR#, XOE#, SUSCLK, RTCX2 **Other Signals:** SMBCLK, SMBDATA, APICACK#, APICCS#, IRQ[0, 8], SPKR, GNT[A:C], GPO[0, 8, 27, 28, 30], IRQ9OUT#
I_{OL4} / I_{OH4}	**PCI Bus Signals:** AD[31:0], C/BE[3:0]#, CLKRUN#, DEVSEL#, FRAME#, IRDY#, PAR, PCIRST#, PHOLD#, SERR#, STOP#, TRDY#, SERIRQ
I_{OL5} / I_{OH5}	**USB Signals:** USBP[1:0]+, USBP[1:0]-
I_{OL6} / I_{OH6}	SMI#, STPCLK#
I_{OL7} / I_{OH7}	INIT#
I_{OL8} / I_{OH8}	SLP#

Table 4. DC Current Characteristics

Functional Operating Range (V_{REF} = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Typ	Max	Unit	Notes
I_{CC}(3 V)	V_{CC} Supply Current	110	155	mA	
I_{CC}(SUS) ON	Suspend Well Supply Current - Full On	3	5	mA	
I_{CC}(SUS) POS/STR	Suspend Well Supply Current - Power On Suspend or Suspend to RAM	30	150	µA	
I_{CC}(SUS) STD/Soff	Suspend Well Supply Current - Suspend to Disk or Soft Off	9	150	µA	
I_{CC}(RTC)	Battery Standby Current	6	8	µA	V_{CC}(RTC) = 3.0 V Mech Off State

2.3 A.C. Characteristics

Table 5. CLOCK/RESET TIMINGS (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figures
PCI Clock Timings						
PCICLK						
t1a	Period	30	33.3	ns		2
t1b	High Time	12.0		ns		2
t1c	Low Time	12.0		ns		2
t1c	Rise Time		3.0	ns		2
t1d	Fall Time		3.0	ns		2
ISA Clock Timings						
SYSCLK						
t1f	Period	120	133.3	ns		2
t1g	High Time	49		ns		2
t1h	Low time	49		ns		2
t1i	RiseTime		4	ns		2
t1j	Fall time		4	ns		2
Oscillator Clock Timings						
OSC						
t1l	OSC Period	67	70	ns		2
t1m	High Time	20				2
t1n	Low time	20		ns		2
USB Clock Timings						
f_{clk48}	Operating Frequency	48		MHz		
t1p	Frequency Tolerance		±2500	ppm	1	2
t1q	High Time	7		ns		2
t1r	Low time	7		ns		2
t1s	Rise Time		1.2	ns		2
t1t	Fall Time		1.2	ns		2
Suspend Clock Timings						

NOTES:
1. The USBCLK is a 48 MHz clock; it expects a 40/60% duty cycle.
2. The maximum high time (t2b Max) provides a simple guaranteed method for devices to detect bus idle conditions.
3. t2j is measured as a transition time through the threshold region V_{ol}=0.8 V and V_{oh}=2.0 V.

Table 5. CLOCK/RESET TIMINGS (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figures
f_{susclk}	SUSCLK Operating Frequency	32		KHz		
t1v	High time	10		µs		
t1w	Low Time	10		µs		
SMBus Clock						
f_{smb}	SMCLK Operating Frequency	10	16	KHz		
t2b	High time	4.0	50	µs	2	40
t2c	Low time	4.7		µs		40
t2d	Clock/Data Rise time		1000	ns		40
t2e	Clock /Data Fall time		300	ns		40
RESET TIMINGS						
t2f	PCIRST#, RSTDRV Driven Inactive After SUS_STATx# is Driven Inactive.		1	RTCCLK		3
t2g	CPURST, PCIRST#, RSTDRV Active Pulse Width. Initiated via the RC Register.	1		ms		4
t2h	CPURST Driven Inactive After PCIRST# is Driven Inactive.		1	RTCCLK		3
t2i	CPURST Valid Delay from PCICLK Rising	2	25	ns		29
t2j	PWROK, RSMRST# Rise time		10	ns	3	
SMI#						
t3a	Valid Delay from PCICLK	2	25	ns		7
t3b	Active Pulse Width	3		PCICLK		5
t3c	Inactive Pulse Width	4		PCICLK		5
EXTSMI#						
t3d	Active Pulse Width	2		PCICLK		5
t3e	Inactive Pulse Width	4		PCICLK		5
t3f	Valid Setup to PCICLK	10		ns		6
t3g	Valid Hold from PCICLK	4		ns		6
STPCLK#						
t3h	Valid Delay from PCICLK	2	25	ns		7
t3i	STPCLK# Inactive Pulse Width	5		PCICLK		5

NOTES:

1. The USBCLK is a 48 MHz clock; it expects a 40/60% duty cycle.
2. The maximum high time (t2b Max) provides a simple guaranteed method for devices to detect bus idle conditions.
3. t2j is measured as a transition time through the threshold region V_{ol}=0.8 V and V_{oh}=2.0 V.

Table 6. PIIX4 as Master Timings (Sheet 1 of 3)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
BALE								
t4a	BALE Pulse Width	50		ns	M,I/O	8,16		8,9,10, 11
t4b	BALE Driven Active from MEMx#, Iox# Inactive	44		ns	M,I/O	8,16		8,9,10, 11
LA[23:17]								
t5a	LA[23:17] Valid Setup to BALE Inactive	150		ns	M	8,16	1	8,9
t5b	LA[23:17] Valid Hold from BALE Inactive	26		ns	M	8,16		8,9
t5c	LA[23:17] Valid Setup to MEMx# Active	150		ns	M	16		9
t5d	LA[23:17] Valid Setup to MEMx# Active	173		ns	M	8		8
t5e	LA[23:17] Invalid from MEMx# Active	39		ns	M	16		9
t5f	LA[23:17] Invalid from MEMx# Active	39		ns	M	8		8
SA[19:0], SBHE#								
t6a	SA[19:0], SBHE# Valid Setup to MEMx# Active	34		ns	M	16	2,3	9
t6b	SA[19:0], SBHE# Valid Setup to Iox# Active	100		ns	I/O	16		11
t6c	SA[19:0], SBHE# Setup to MEMx#, Iox# Active	100		ns	M,I/O	8		8, 10
t6d	SA[19:0], SBHE# Valid Setup to BALE Inactive	37		ns	M,I/O	8,16	2,3	8,9,10, 11
t6e	SA[19:0], SBHE# Valid Hold from MEMx#, Iox# Inactive	41		ns	M,I/O	8,16		8,9,10, 11
MEMR#, MEMW#, IOR# and IOW#								
t7a	MEMx# Active Pulse Width (std)	225		ns	M	16		9
t7b	Iox# Active Pulse Width (std)	160		ns	I/O	16		11
t7c	MEMx# Active Pulse Width (nws)	105		ns	M	16	4	9
t7d	MEMx# or Iox# Active Pulse Width (std)	520		ns	M,I/O	8		8,10
t7e	MEMx# or Iox# Active Pulse Width (nws)	160		ns	M,I/O	8	4	8,10
t7f	MEMx# Inactive Pulse Width	103		ns	M	16		9
t7g	MEMx# Inactive Pulse Width	163		ns	M	8		8
t7h	Iox# Inactive Pulse Width	163		ns	I/O	8,16		10,11

NOTES:
1. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
2. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices should not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
3. For back-to-back “sub cycles” generated as a result of byte assembly or disassembly, this specification is 34 ns.
4. No-wait-state (ZEROWS#) asserted.

Table 6. PIIX4 as Master Timings (Sheet 2 of 3)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
t7i	MEMx#, Iox# Driven Inactive from IOCHRDY Active	120		ns	M,I/O	8,16		8,9,10, 11
SMEMR# and SMEMW#								
t8a	SMEMR# & SMEMW# Propagation Delay from MEMR# and MEMW#		16	ns	M	8,16		8,9
Read Data								
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O	8,16		8,9,10, 11
t9b	Read Data Valid Setup to MEMR#, IOR#	24		ns	M,I/O	8,16		8,9,10, 11
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		8,9,10, 11
t9d	Read Data three stated from MEMR# and IOR# Inactive		41	ns	M,I/O	8,16		8,9,10, 11
Write Data								
t10a	Write Data Valid Setup to MEMW# Active Write Data Valid Setup to IOW# Active Write Data Valid Setup to IOW# Active	-40 -40 +23		ns ns ns	M,I/O M,I/O M,I/O	8,16 8 16		8,9,10, 11
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O	8,16		8,9,10, 11
t10c	Write Data three stated from MEMW#, IOW# Inactive		105	ns	M,I/O	8,16		8,9,10, 11
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O	8,16		8,9,10, 11
MEMCS16#								
t11a	MEMCS16# Driven Active from LA[23:17] Valid		94	ns	M	16		9
t11b	MEMCS16# Inactive from LA[23:17] Valid		91	ns	M	8		8
t11c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		9
t11d	MEMCS16# Driven Active from SA[19:2] Valid		35	ns	M	16		9
IOCS16#								
t12a	IOCS16# Driven Active from Valid SA[19:0]		123	ns	I/O	16		11
t12b	IOCS16# Inactive from Valid SA[19:0]		91	ns	I/O	8		10

NOTES:
1. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
2. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices should not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
3. For back-to-back “sub cycles” generated as a result of byte assembly or disassembly, this specification is 34 ns.
4. No-wait-state (ZEROWS#) asserted.

Table 6. PIIX4 as Master Timings (Sheet 3 of 3)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
t12c	IOCS16# Valid Hold from SA[19:0] Invalid	0		ns	I/O	16		11
t12d	IOCS16# Driven Active from Iox Active		80	ns	I/O	16		11
ZEROWS#								
t13a	ZEROWS# Driven Active from MEMx# Active		16	ns	M	16		9
t13b	ZEROWS# Driven Active from MEMx#, Iox# Active		80	ns	M,I/O	8		8, 10
t13c	ZEROWS# Driven Active from LA[23:17] Valid		180	ns	M	16		9
t13d	ZEROWS# Driven Active from LA[23:17] Valid		300	ns	M	8		8
ZEROWS#								
t13e	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		80	ns	M	16		9
t13f	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		200	ns	M,I/O	8		8,10
AEN								
t14a	AEN Valid Setup to Iox# Driven Active	111		ns	I/O	8,16		10,11
t14b	AEN Valid Setup to BALE Driven Inactive	111		ns	I/O	8,16		10,11
t14c	AEN Valid Hold from Iox# Driven Inactive	41		ns	I/O	8,16		10,11
IOCHRDY								
t15a	IOCHRDY Driven Valid from MEMx#, Iox# Active		78	ns	M,I/O	16		9,11
t15b	IOCHRDY Driven Valid from MEMx#, Iox# Active		366	ns	M,I/O	8		8,10
t15e	IOCHRDY Inactive Pulse Width	0.12	15.6	µs	M,I/O	8,16		8,9,10, 11

NOTES:

1. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
2. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices should not use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
3. For back-to-back “sub cycles” generated as a result of byte assembly or disassembly, this specification is 34 ns.
4. No-wait-state (ZEROWS#) asserted.

Table 7. PIIX4 as Slave Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Figure
LA[23:17]								
t16a	LA[23:17] Valid Setup to MEMx# Active	23		ns	M	16		12
SA[19:0],SBHE#								
t17a	SA[19:0],SBHE# Setup to MEMx# Active	23		ns	M	16		12
t17b	SA[19:0],SBHE# Setup to Iox# Active	89		ns	I/O	8		13
t17c	SA[19:0],SBHE# Valid Hold from MEMx#, Iox# Inactive	30		ns	M,I/O	8,16		12,13
MEMR#, MEMW#, IOR#, IOW#								
t18a	MEMx# Active Pulse Width	214		ns	M	16		12
t18b	Iox# Active Pulse Width	509		ns	I/O	8		13
t18c	MEMx# Inactive Pulse Width	92		ns	M	16		12
t18d	Iox# Inactive Pulse Width	152		ns	I/O	8		13
Read Data								
t19a	Read Data Valid from IOCHRDY Active		69	ns	M,I/O	8,16		12,13
t19b	Read Data Valid from IOR# Active		69	ns	I/O	8	1	13
t19c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		12,13
t19d	Read Data Three State from MEMR#, IOR# Inactive		55	ns	M,I/O	8,16		12,13
Write Data								
t20a	Write Data Valid Setup to MEMW#, IOW# Active	-54		ns	M,I/O	8,16		12,13
t20b	Write Data Valid Hold from MEMW#, IOW# Inactive	14		ns	M,I/O	8,16		12,13
MEMCS16#								
t21a	MEMCS16# Driven Active from Valid LA[23:17]		65	ns	M	16		12
t21b	MEMCS16# Float from Valid LA[23:17]		31	ns	M	16		12
t21c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		12
IOCHRDY								
t22a	IOCHRDY Inactive from MEMx#, Iox# Active		50	ns	M,I/O	8,16		12,13
t22b	IOCHRDY Float from IOCHRDY Rising		85	ns	M,I/O	8,16	2	12,13
t22c	IOCHRDY Inactive Pulse Width	0.12	2.5	µs	M,I/O	8,16		12,13

NOTES:

1. This applies to the PIIX4 cycles that IOCHRDY is not driven low.
2. This specification includes both the time the PIIX4 drives IOCHRDY active and the time it takes the PIIX4 to float IOCHRDY.

Table 8. Interrupt and NMI Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Figure
NMI Timing					
t23a	SERR#, IOCHK# Active to NMI Driven Active		200	ns	14
Interrupt Timing					
t24a	IRQx Inactive Pulse Width	100		ns	15

Table 9. ISA Bus Master Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
DACK#						
t26a	DACK#, Inactive from DREQ Inactive	240		ns		16
Three Stating and Driving the Bus						
t27a	PIIX4 Three States Address, Data, and Control Signals from DACK#, Active		30	ns		16
t27b	PIIX4 Drives Address, Data, and Control Signals from DACK#, Inactive	71		ns		16
SMEMR# and SMEMW#						
t28a	SMEMR# and SMEMW# Active (falling edge) from MEMR# and MEMW# Active (falling edge)		25	ns		16
t28b	SMEMR# and SMEMW# Inactive (rising edge) from MEMR# and MEMW# Inactive (rising edge)		35	ns		16
Data Swap Logic Timing (ISA Master to ISA slave)						
t29a	SD[7:0] to SD[15:8] Propagation Delay		26	ns		17
t29b	SD[15:8] to SD[7:0] Propagation Delay		26	ns		17
t29c	PIIX4 Drives Data Bus from IOR#, IOW#, MEMR# or MEMW# Active		26	ns	1	17
t29d	PIIX4 Three States Bus from IOR#, MEMR#, or SMEMR# Inactive	2	55	ns	1,2	17
t29e	PIIX4 Three States Bus from IOW#, MEMW#, or SMEMW# Inactive	2	60	ns	1,2	17

NOTES:

1. This applies to the byte lane that the data has been swapped to.
2. Data is three stated from the standard memory commands (SMEMR# or SMEMW#), when they are generated.

Table 10. DMA Compatible Timings (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
DREQ						
t30a	DREQ Active Hold from IOR# Active		558	ns	1	19
t30b	DREQ Active Hold from IOW# Active		315	ns	1	18
DACK#						
t31a	DACK# Active to IOR# Active	73		ns		19
t31b	DACK# Active to IOW# Active	312		ns		18
t31c	DACK# Active Hold from IOR# Inactive	100		ns		19
t31d	DACK# Active Hold from IOW# Inactive	155		ns		18
AEN and BALE						
t32a	AEN Active to Iox# Active	111		ns		18,19
t32b	AEN and BALE Inactive from Iox# Inactive	41		ns		18,19
LA[23:19], SA[19:0], SBHE#						
t33a	LA[23:19],SA[19:0], SBHE# Valid Setup to MEMx# Active	99		ns		18,19
t33b	LA[23:19],SA[19:0], SBHE# Valid Hold from MEMx# Inactive	51		ns		18,19
MEMR#, MEMW#, IOR#, IOW#						
t34a	IOW# and MEMW# Active Pulse Width	465		ns		18,19
t34b	MEMR# Active Pulse Width	495		ns		18
t34c	IOR# Active Pulse Width	760		ns		19
t34d	IOW# Inactive Pulse Width (continuous)	465		ns		18
t34e	IOR# Inactive Pulse Width (continuous)	160		ns		19
t34f	IOR# Active to MEMW# Active	230		ns		19
t34g	MEMR# Active to IOW# Active	-26		ns		18
t34h	MEMR# Active Hold from IOW# Inactive	40		ns		18
t34i	IOR# Active Hold from MEMW# Inactive	40		ns		19
t34j	MEMx# Active Hold from IOCHRDY Active	120		ns		18,19
SMEMR# & SMEMW#						
t35a	SMEMR# & SMEMW# Valid from MEMR# and MEMW# Valid		15	ns		18,19
Read Data						
t36a	Read Data Valid from IOR# Active		237	ns		19
t36b	Read Data Valid Hold from IOR# Inactive	0		ns		19
t36c	Read Data Float from IOR# Inactive		61	ns		19
Write Data						

NOTES:
1. This applies to the last cycle of a demand mode DMA transfer.
2. This applies to the byte lane that the data has been swapped to.
3. Output from PIIX4.

Table 10. DMA Compatible Timings (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
t37a	Write Data Valid Setup to IOW# Inactive	225		ns		18
t37b	Write Data Valid Hold from IOW# Inactive	36		ns		18
Data Swap Logic Timing (ISA to ISA Transaction)						
t38a	SD[7:0] to SD[15:8] Propagation Delay		26	ns		20
t38b	SD[15:8] to SD[7:0] Propagation Delay		26	ns		20
t38c	PIIX4 Drives Data Bus from IOR# or MEMR# Active		26	ns	2	20
t38d	PIIX4 Three States Bus from IOR# or MEMR# Inactive		55	ns	2	20
TC						
t39a	TC Active Setup to Iox# Inactive	511		ns	3	18,19
t39b	TC Active Hold from Iox# Inactive	71		ns	3	18,19
t39h	TC Pulse Width	700		ns		18,19
IOCHRDY						
t40b	IOCHRDY Valid from MEMx# Active		315	ns		18,19
t40c	IOCHRDY Inactive Pulse Width	125		ns		18,19

NOTES:

1. This applies to the last cycle of a demand mode DMA transfer.
2. This applies to the byte lane that the data has been swapped to.
3. Output from PIIX4.

Table 11. DMA Type "F" Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
DREQ						
t55a	DREQ Active Hold from IOR# Active		82	ns	1, 2	21
t55b	DREQ Active Hold from IOW# Active		82	ns	1, 2	21
DACK#						
t56a	DACK# Active to IOR# Active	77		ns	2	21
t56b	DACK# Active to IOW# Active	77		ns	2	21
t56c	DACK# Active Hold from IOR# Inactive	30		ns	2	21
t56d	DACK# Active Hold from IOW# Inactive	30		ns	2	21
AEN and BALE						
t57a	AEN Active to Iox# Active	111		ns		21
t57b	AEN and BALE Inactive from Iox# Inactive	41		ns		21
IOR# and IOW#						
t58a	IOR# Active Pulse Width	110		ns		21
t58b	IOW# Active Pulse Width	110		ns		21
t58c	IOR# Inactive Pulse Width (Continuous)	115		ns		21
t58d	IOW# Inactive Pulse Width (Continuous)	115		ns		21
Read Data						
t59a	Read Data Valid from IOR# Active		96	ns		21
t59b	Read Data Valid Hold from IOR# Inactive	2		ns		21
t59c	Read Data Float from IOR# Inactive		61	ns		21
Write Data						
t60a	Write Data Valid Setup to IOW# Inactive	70		ns		21
t60b	Write Data Valid Hold from IOW# Inactive	31		ns		21
TC						
t61a	TC Active Setup to IOR# Inactive	40		ns	3	21
t61b	TC Active Setup to IOW# Inactive	40		ns	3	21
t61c	TC Active Hold from Iox# Inactive	0		ns	3	21

NOTES:

1. This applies to the last cycle of a demand mode DMA transfer.
2. Type F transfers are selected via the MBDMAX Register.
3. Output from PIIX4.

Table 12. ISA Refresh Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
REFRESH#						
t62a	REFRESH# Active Setup to MEMR# Active	120		ns		22,23
t62b	REFRESH# Active Hold from MEMR# Inactive	31	260	ns		22,23
t62c	REFRESH# Driven Active to SA[15:0] Valid	11		ns		22,23
t62d	REFRESH# Active Hold from SA[15:0] Invalid	11		ns		22,23
AEN						
t63a	AEN Driven Active to MEMR# Active	11		ns		22,23
t63b	AEN Hold from MEMR# Inactive	11		ns		22,23
SA[15:0]						
t64a	SA[15:0] Valid Setup to MEMR# Active	72		ns		22,23
t64b	SA[15:0] Valid Hold from MEMR# Inactive	35		ns		22,23
t64c	SA[15:0] Valid Float from MEMR# Inactive	46	120	ns	1	23
MEMR#, SMEMR#						
t65a	MEMR# Active Pulse Width	225		ns		22,23
t65b	MEMR# Three state from MEMR# Inactive	36	120	ns		22,23
t65c	MEMR# Driven Inactive from IOCHRDY Active	120		ns		22,23
t65d	SMEMR# Propagation Delay from MEMR#		25	ns		22,23
IOCHRDY						
t66a	IOCHRDY Inactive from MEMR# Active		76	ns		22,23
t66b	IOCHRDY Valid from MEMR# Active		76	ns		22,23
t66c	IOCHRDY Inactive Pulse Width	120		ns		22,23
PIIX4 Driving Bus From REFRESH#						
t67a	PIIX4 Drives Control and Address from REFRESH# Active	5		ns	1	23

NOTE:

1. This applies to ISA Master initiated refresh only.

Table 13. PIIX4 and ISA Master Accesses to the X-Bus

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
BIOSCS#, KBCCS#, RTCCS#, AND PCS0#, PCS1#, MCCS#						
t68a	CS# Driven Active from SA[19:0], LA[23:17] Valid (except BIOSCS#)		35	ns		24
t68b	CS# Driven Inactive from SA[16:0], LA[23:17] Invalid (except BIOSCS#)		35	ns		24
XDIR# and XOE#						
t69a	XDIR# Active from IOR#, MEMR# Active - PCI-Initiated Access - ISA-Initiated Access		 25 30	 ns ns		24
t69b	BIOSCS#, XOE# Active from Iox#, MEMx# Active		29	ns		24
t69c	XDIR# Active Setup to XOE# Active	2	12	ns		24
t69d	BIOSCS#, XOE# Inactive from Iox#, MEMx# Inactive	35	60	ns	1	24
t69f	BIOSCS#, XOE# Setup to XDIR# Inactive	2	15	ns	1	24
t69g	XOE# Inactive from IOR#, MEMR# Inactive	2	140	ns	2	24
t69i	XOE# Inactive Setup to XDIR# Inactive	2	12	ns	2	24

NOTES:

1. PIIX4 as a master cycles only.
2. ISA master cycles only.

Table 14. Miscellaneous X-Bus Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
Mouse Timing Support						
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns		25
Coprocessor Error Support						
t73a	IGNNE# Active from IOW# Active from Port F0H Access		220	ns		25
t73b	IGNNE# Inactive from FERR# Inactive		230	ns		25
Real Time Clock Timing (RTCALE)						
t75a	RTCALE Pulse Width	200	300	ns		26
t75b	RTCALE Active from IOW# Active - PCI-Initiated Access - ISA-Initiated Access		 85 156	 ns ns		26
Speaker Timing						
t76a	SPKR Valid Delay from OSC Rising		200	ns		27

Table 15. PCI Interface Timing

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
t77	AD[31:0] Valid Delay	2	11	ns	Min: 0 pF Max: 50 pF	29
t78	AD[31:0] Setup Time	7		ns		30
t79	AD[31:0] Hold Time	0		ns		30
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# CLOCKRUN#, GNT[A:C]# Valid Delay from PCICLK Rising	2	11	ns	Min: 0 pF Max: 50 pF	29
t81	C/Bes[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# CLOCKRUN#, GNT[A:C]# Output Enable Delay from PCICLK Rising	2		ns		33
t82	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# CLOCKRUN#, Float Delay from PCICLK Rising	2	28	ns		31
t83	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# CLOCKRUN#, REQ[A:C]# Setup Time to PCICLK Rising	7		ns		30
t84	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL# CLOCKRUN#, REQ[A:C]#, Hold Time from PCLKIN Rising	0		ns		30
t85	PHLD# Valid Delay from PCICLK Rising	2	12	ns	0 pF	29
t86	PHLDA# Setup Time to PCICLK Rising	10		ns		30
t87	PHLDA# Hold Time from PCICLK Rising	0		ns		30
t91	PIRQ[D:A]# Setup Time to PCICLK Rising				1	30
t92	PIRQ[D:A]# Hold Time From PCICLK Rising				1	30
t96	RST# Low Pulse Width	1		ms		32

NOTE:

1. This signal is internally synchronized.

Table 16. PCI Bus IDE Timing (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Figure
Primary IDE Timing						
t102	PDIOW# Active From PCICLK Rising	2	20	ns		35
t103	PDIOW# Inactive From PCICLK Rising	2	20	ns		34,35
t104	PDIOR# Active From PCICLK Rising	2	20	ns		35
t105	PDIOR# Inactive From PCICLK Rising	2	20	ns		34,35
t106	PDA[2:0] Valid Delay From PCICLK Rising	2	30	ns		34
t107	PDCS1#, PDCS3# Active From PCICLK Rising	2	30	ns		34
t108	PDCS1#, PDCS3# Inactive From PCICLK Rising	2	30	ns		
t113	PDDACK# Active From PCICLK Rising	2	20	ns		35
t114	PDDACK# Inactive From PCICLK Rising	2	20	ns		
t114a	PDDREQ Setup Time to PCICLK Rising	7		ns		35
t114b	PDDREQ Hold From PCICLK Rising	7		ns		35
t115	PDD[15:0] Valid Delay From PCICLK Rising	2	30	ns		34,35
t115a	PDD[15:0] Setup Time to PCICLK Rising	10		ns		34,35
t115b	PDD[15:0] Hold From PCICLK Rising	8		ns		34,35
t116	PIORDY Setup Time to PCICLK Rising	7		ns	1	34
t117	PIORDY Hold From PCICLK Rising	7		ns	1	34
t117a	PIORDY Inactive Pulse Width	48		ns		34
t118	PIORDY Sample Point From DIOx# Assertion			PCICLK	2, 3	34
t119	PDIOx# Active Pulse Width			PCICLK	2, 3	34,35
t120	PDIOx# Inactive Pulse Width			PCICLK	3, 4	34,35
Secondary IDE Timing						
t102	SDIOW# Active From PCICLK Rising	2	20	ns		35
t103	SDIOW# Inactive From PCICLK Rising	2	20	ns		34,35
t104	SDIOR# Active From PCICLK Rising	2	20	ns		35
t105	SDIOR# Inactive From PCICLK Rising	2	20	ns		34,35
t106	SDA[2:0] Valid Delay From PCICLK Rising	2	30	ns		34

NOTES:

1. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
2. This parameter is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register.
3. The cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. This parameter is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 16. PCI Bus IDE Timing (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

t107	SDCS1#, PDCS3# Active From PCICLK Rising	2	30	ns		34
t108	SDCS1#, PDCS3# Inactive From PCICLK Rising	2	30	ns		
t113	SDDACK# Active From PCICLK Rising	2	20	ns		35
t114	SDDACK# Inactive From PCICLK Rising	2	20	ns		
t114a	SDDREQ Setup Time to PCICLK Rising	7		ns		35
t114b	SDDREQ Hold From PCICLK Rising	7		ns		35
t115	SDD[15:0] Valid Delay From PCICLK Rising	2	30	ns		34,35
t115a	SDD[15:0] Setup Time to PCICLK Rising	10		ns		34,35
t115b	SDD[15:0] Hold From PCICLK Rising	8		ns		34,35
t116	SIORDY Setup Time to PCICLK Rising	7		ns	1	34
t117	SIORDY Hold From PCICLK Rising	7		ns	1	34
t117a	PIORDY Inactive Pulse Width	48		ns		34
t118	SIORDY Sample Point From DIOx# Assertion			PCICLK	2, 3	34
t119	SDIOx# Active Pulse Width			PCICLK	2, 3	34,35
t120	SDIOx# Inactive Pulse Width			PCICLK	3, 4	34,35

NOTES:

1. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
2. This parameter is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register.
3. The cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. This parameter is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 17. Universal Serial Bus Timings (Sheet 1 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
Full Speed Source (Note 7)						
t122	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	36
t123	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	36
t124	Source Differential Driver Jitter - To Next Transition - For Paired Transitions	 -2 -1	 2 1	 ns ns	2, 3	37
t125	Source EOP Width	160	175	ns	4	38
t126	Differential to SE0 Transition Skew	-2	5	ns	5	
t127	Receiver Data Jitter Tolerance - To Next Transition - For Paired Transitions	 -20 -10	 20 10	 ns ns	3	37
t128	EOP Width - Must reject as EOP - Must accept as EOP	 40 85		 ns ns	4	38
t126	Differential to SE0 Transition Skew	-2	5	ns	5	
Low Speed Source (Note 8)						
t127	USBPx+, USBPx- Driver Rise Time	 75	 300	 ns ns	1, 6 = 50 pF C_L = 350 pF	36
t128	USBPx+, USBPx- Driver Fall Time	 75	 300	 ns ns	1, 6 C_L = 50 pF C_L = 350 pF	36
t129	Source Differential Driver Jitter - To Next Transition - For Paired Transitions	 -2 -1	 2 1	 ns ns	2, 3	37

NOTES:
1. Driver output resistance under steady state drive is specified at 28 ohms at minimum and 43 ohms at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

Table 17. Universal Serial Bus Timings (Sheet 2 of 2)

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t130	Source EOP Width	160	175	ns	4	38
t131	Differential to SE0 Transition Skew	-2	5	ns	5	
t132	Receiver Data Jitter Tolerance - To Next Transition - For Paired Transitions	 -20 -10	 20 10	 ns ns	3	37
t133	EOP Width - Must reject as EOP - Must accept as EOP	 40 85		 ns ns	4	38
t134	Differential to SE0 Transition Skew	-2	5	ns	5	

NOTES:

1. Driver output resistance under steady state drive is specified at 28 ohms at minimum and 43 ohms at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps.
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps.

Table 18. IOAPIC Bus Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t136	APICCS# Setup to MEMx#	2		PCICLK	1	39
t137	SA[19:0] Setup to APICCS#	2		PCICLK	1	39
t138	APICACK# Valid Delay from PCICLK	2.0	12.0	ns		29
t139	APICREQ# Valid Setup to PCICLK	10.0		ns		30
t140	APICREQ# Valid Hold from PCICLK	0.0		ns		30

NOTE:

1. With these exceptions, the APIC configuration cycles conform to the 8-bit ISA Memory Slave Timing where PIIX4 is the master.

Table 19. SMBUS Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t141	Bus free time between Stop and Start Condition	4.7		µs		40
t142	Hold time after (repeated) Start Condition. After this period, the first clock is generated	4.0		µs		40
t143	Repeated Start Condition setup time	4.7		µs		40
t144	Stop Condition setup time	4.0		µs		40
t145	Data hold time	300		ns		40
t146	Data setup time	250		ns		40
t147	Device time out	25	35	ms	1	
t148	Cumulative clock low extend time (slave device)		25	ms	2	41
t149	Cumulative clock low extend time (master device)		10	ms	3	41

NOTES:

1. A device will timeout when any clock low exceeds this value.
2. t148 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t149 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-acknowledge, acknowledge-to-acknowledge, or acknowledge-to-stop.

Table 20. Serial IRQ Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t151	SERIRQ Setup Time to PCICLK Rising	7		ns		30
t152	SERIRQ Hold Time from PCICLK Rising	0		ns		30

Table 21. ULTRADMA/33 Timings

Functional Operating Range (VREF = 5 V ± 5%, V_{CC} = 3.3 V ± 0.3 V, T_{CASE} = 0° C to +85° C)

		Mode 0 (ns)		Mode 1 (ns)		Mode 2 (ns)		
Sym	**Parameter (Note 1)**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Figure**
t154	Cycle Time (Tcyc) (Note 2)	114		75		55		43
t155	Two Cycle Time (T2cyc)	235		156		117		43
t156	Data Setup Time (Tds)	15		10		7		43
t157	Data Hold Time (Tdh)	5		5		5		43
t158	Data Valid Setup Time (Tdvs)	70		48		34		43
t159	Data Valid Hold Time (Tdvh)	6		6		6		43
t160	Limited Interlock Time (Tli)	0	150	0	150	0	150	45
t161	Interlock Time w/ Minimum (Tmli)	20		20		20		45
t162	Envelope Time (Tenv)	20	70	20	70	20	70	42
t163	Ready to pause Time (Trp)	160		125		100		44
t164	DMACK setup/hold Time (Tack)	20		20		20		42,45

NOTES:

1. The specification symbols in parenthesis correspond to the Ultra DMA/33 specification name.
2. These cycle timings are based on the STOBE period as indicated in Figure 44. However, Table 13 in the PIIX4 datasheet refers to cycle time strobe periods as 120 ns, 90 ns and 60 ns for mode 0, 1, and 2 respectively. The datasheet timings are different because they are based on the number of PCI clocks per cycle, not the actual period between the rise and fall of STROBE.

Table 22. AC Test Loads

Capacitive Load	Signals
120 pf	REFRESH#, TC, SD[15:0], SA[19:0], SBHE#, LA[23:17], I0CS16#, MEMCS16#, MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW#, AEN, BALE, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK
50 pf	DACK#[7:5,3:0], SPKR, INTR, NMI, BIOSCS#, KBCCS#, RTCCS#, PCS[1:0]#, MCCS#, RTCALE, XDIR#, XOE#, IGNNE#, PDD[15:0], SDD[15:0], APICCS#, DIOR#, DIOW#, PDDACK#, SDDACK#, #, PDCS1# PDCS3#, SDCS1#, SDCS3##, PDA[2:0], SDA[2:0].

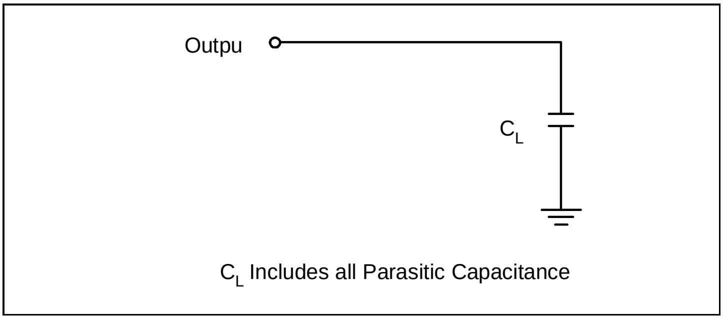

Figure 1. Test Load

2.4 Clock, Reset, ISA Bus, X-Bus, and Host Timing Diagrams

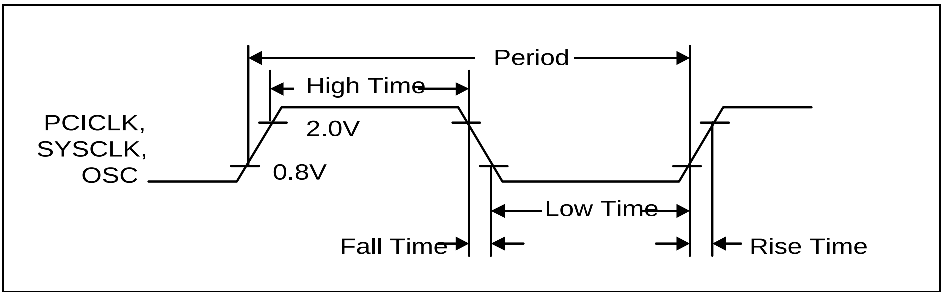

Figure 2. Clock Timing

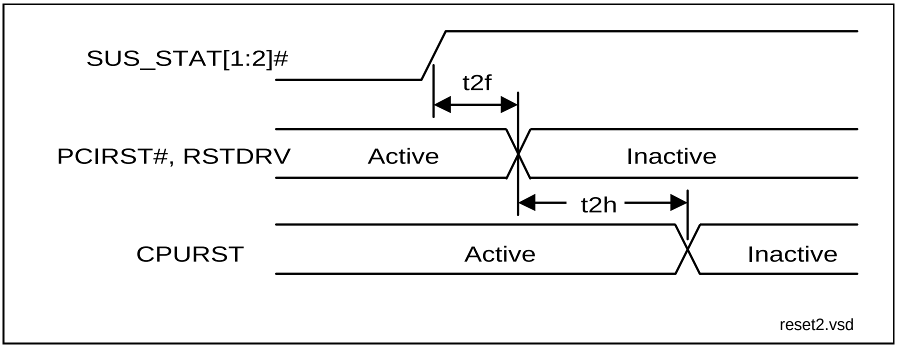

Figure 3. Reset Inactive Timing

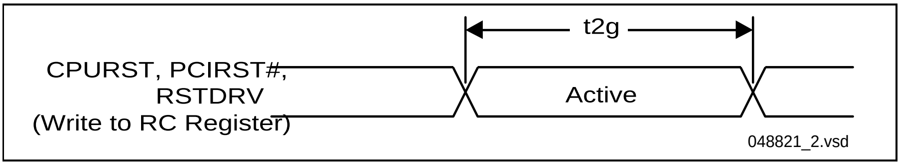

Figure 4. Reset Active Pulse Width

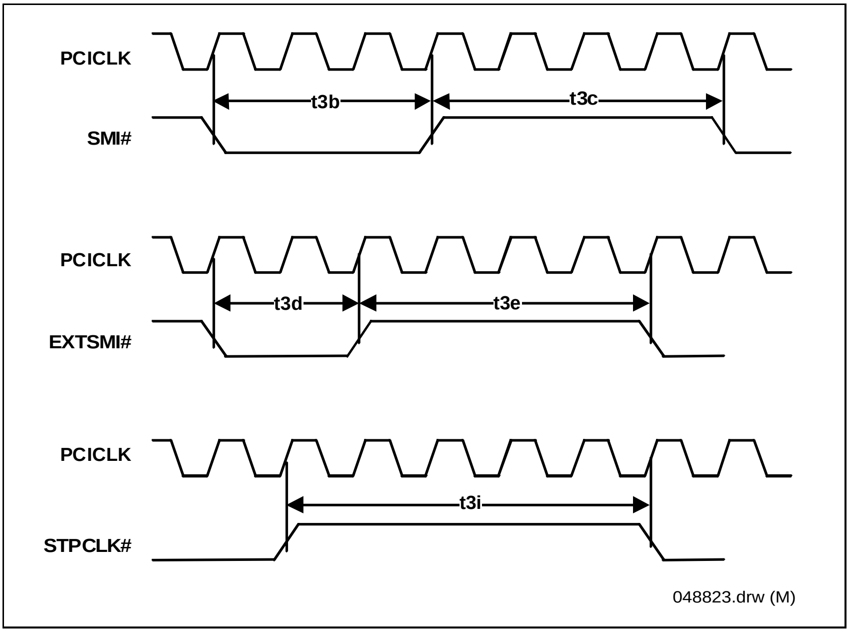

Figure 5. SMI#, EXTSMI#, and STPCLK# Timing

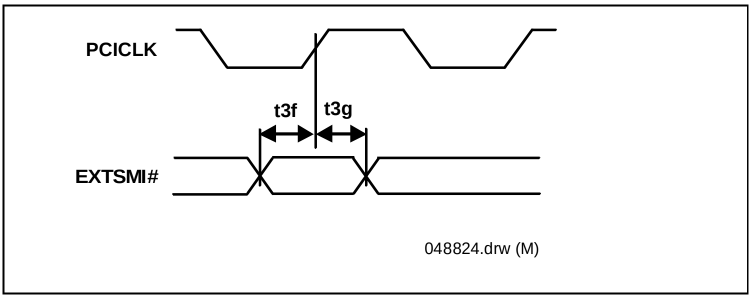

Figure 6. Input to PCICLK Setup/Hold Times

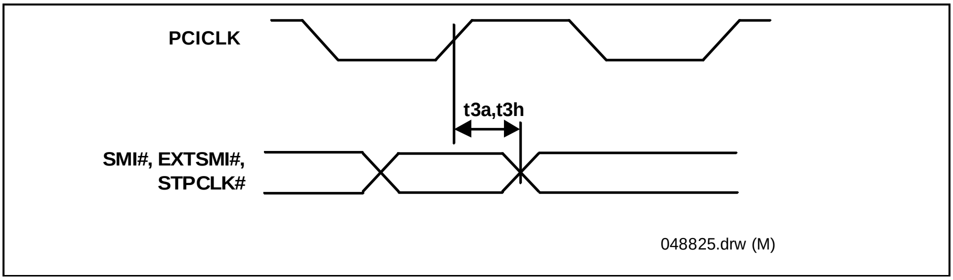

Figure 7. HCLKIN to Output Valid Delay

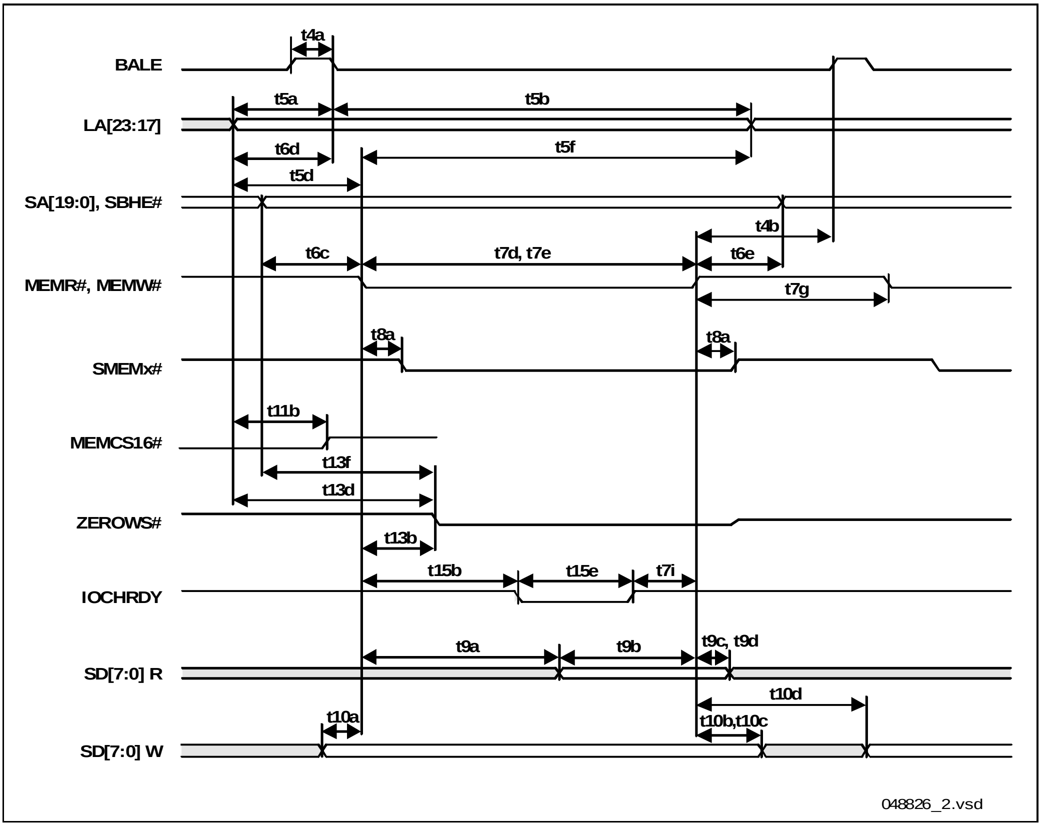

Figure 8. 8-Bit ISA Memory Slave Timing (PIIX4 as Master)

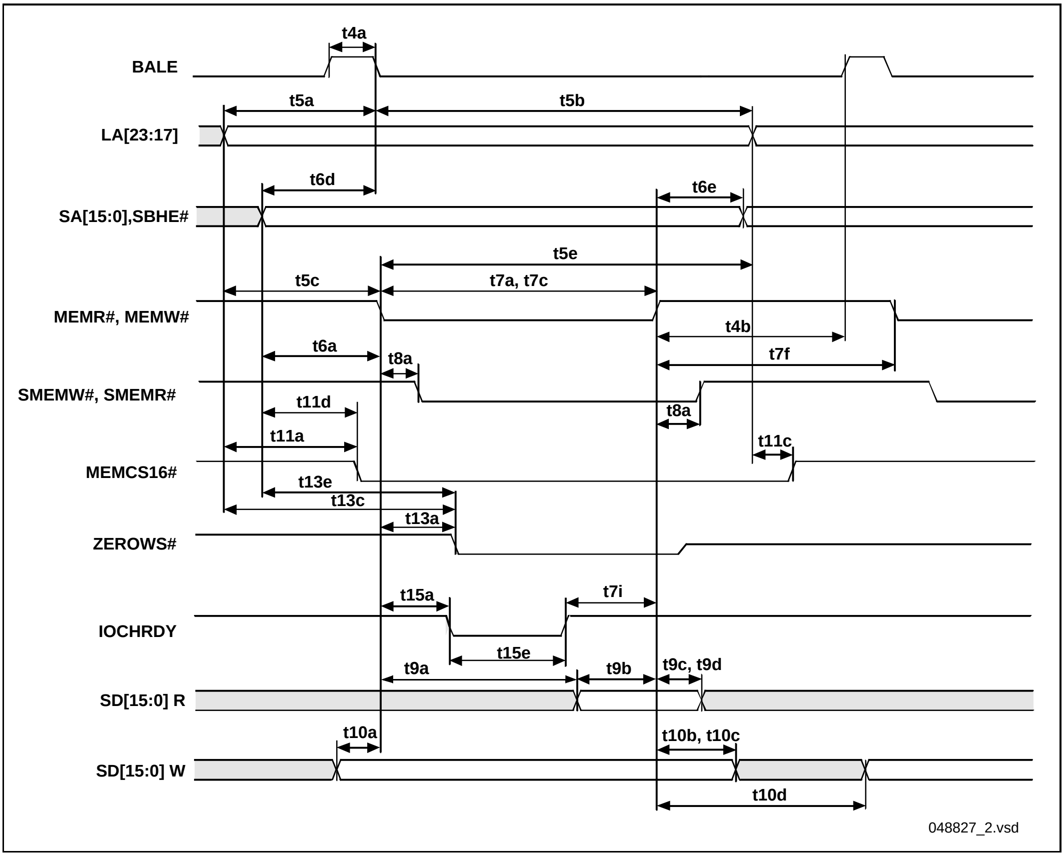

Figure 9. 16-Bit ISA Memory Slave Timing (PIIX4 as Master)

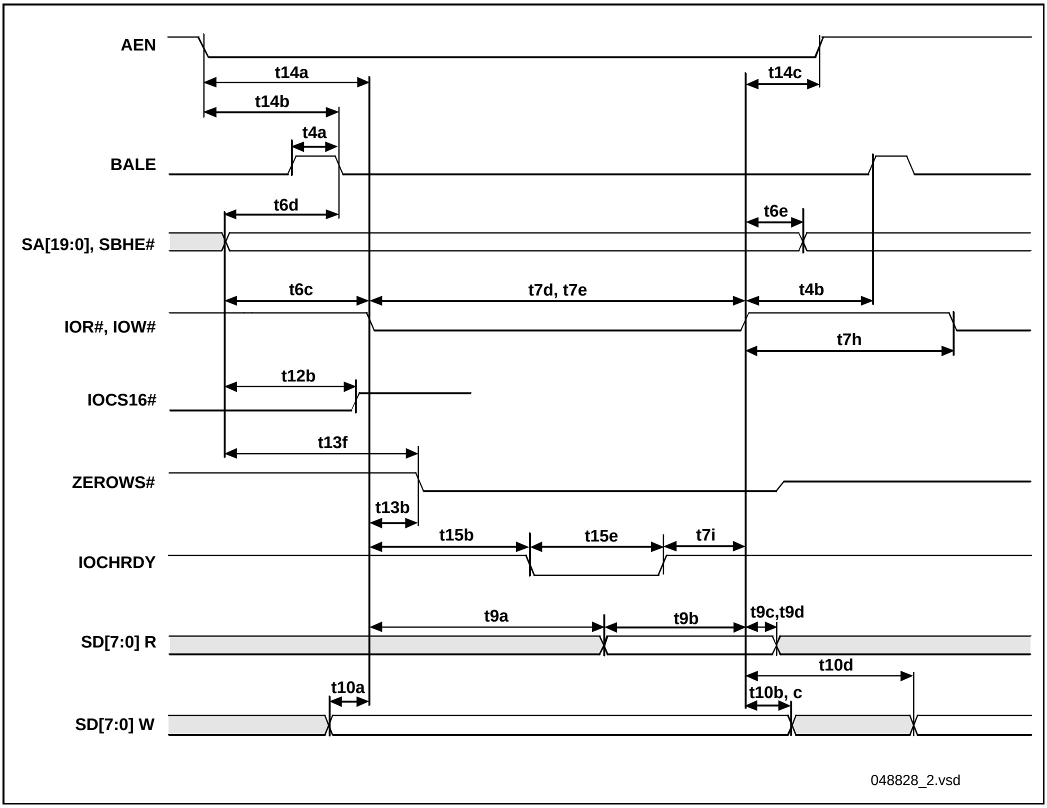

Figure 10. 8-Bit ISA I/O Slave Timing (PIIX4 as Master)

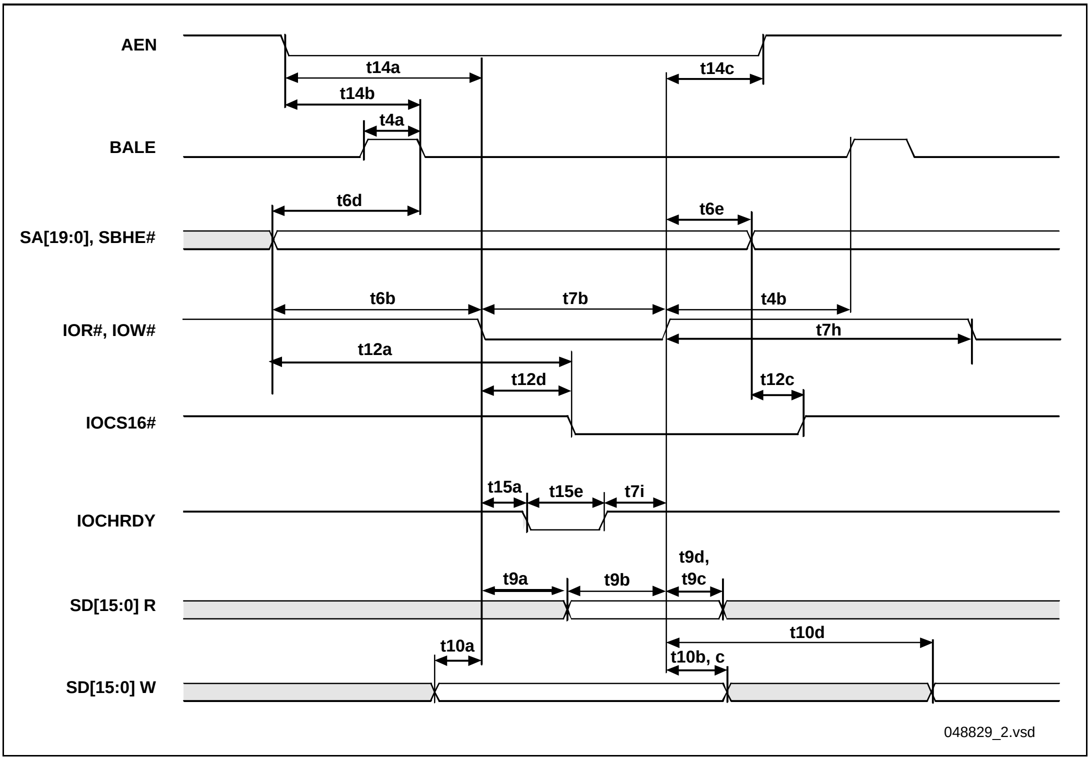

Figure 11. 16-Bit I/O Slave Timing (PIIX4 as Master)

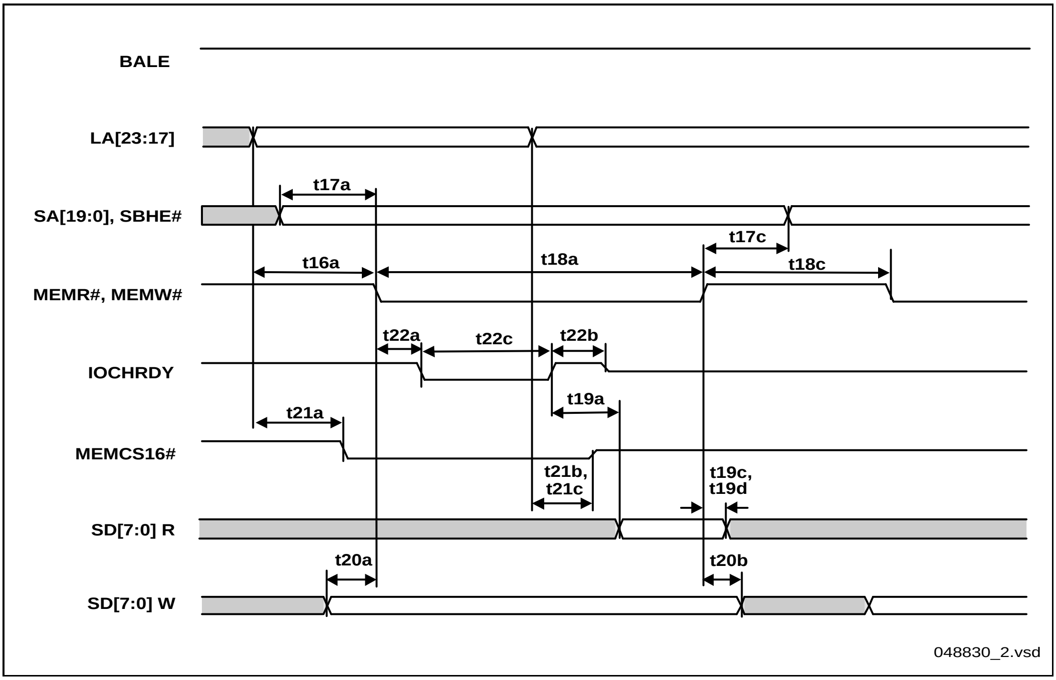

Figure 12. ISA Master Accessing PCI Memory Timing

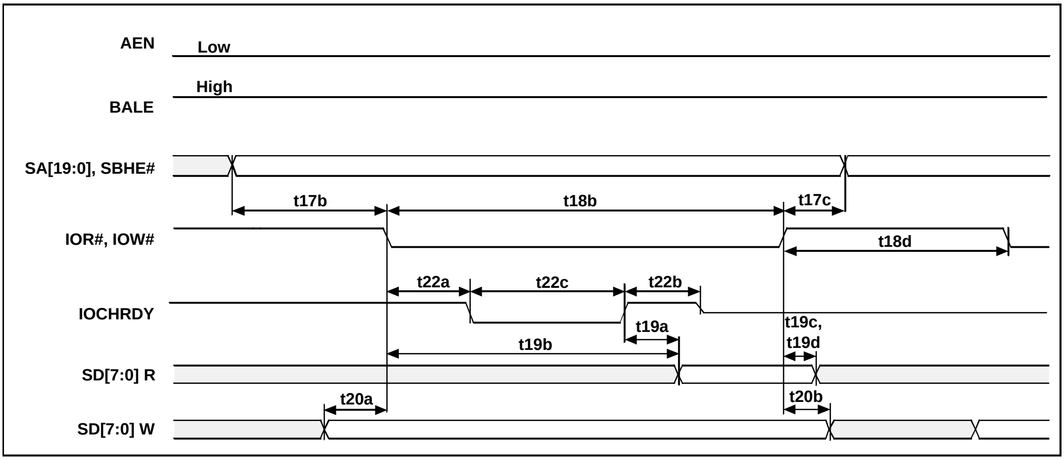

Figure 13. ISA Master Accessing PIIX4 Register Timing

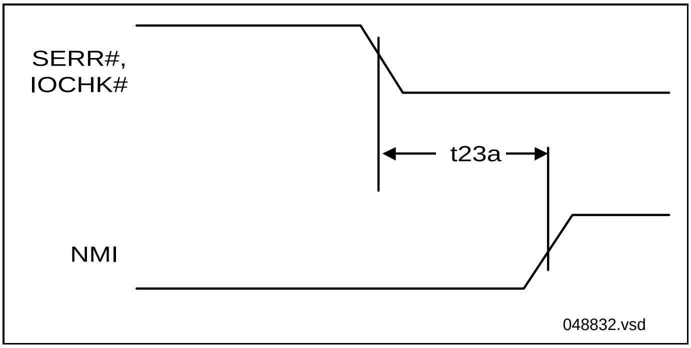

Figure 14. NMI Timing

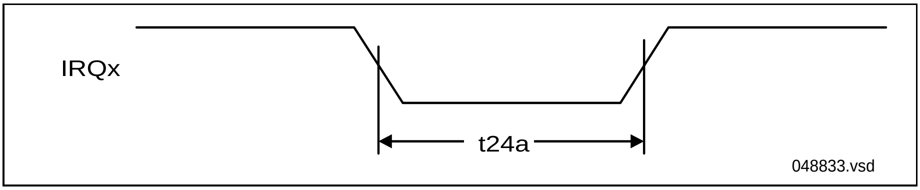

Figure 15. Interrupt Timing

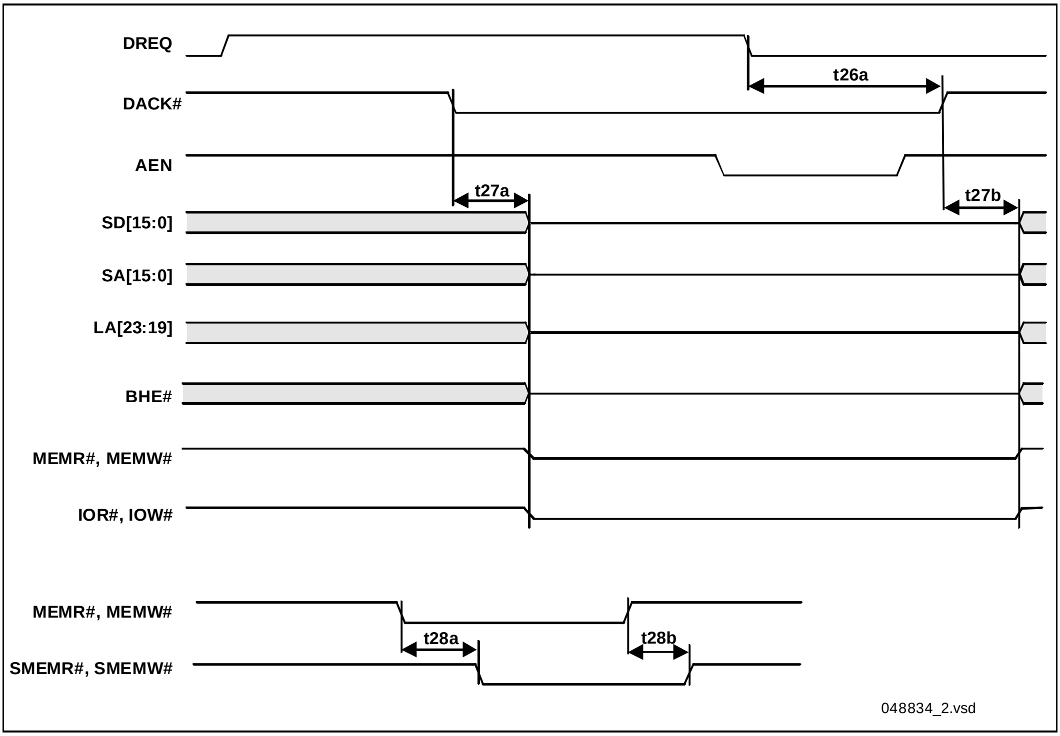

Figure 16. ISA Master Miscellaneous Timing

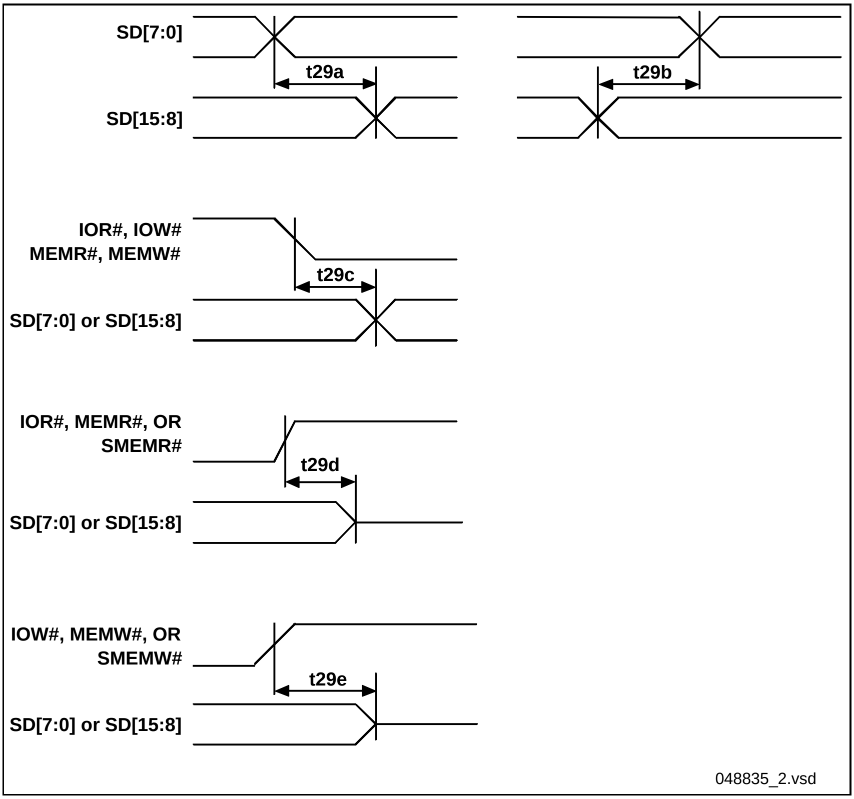

Figure 17. ISA Master Data Swap Timing

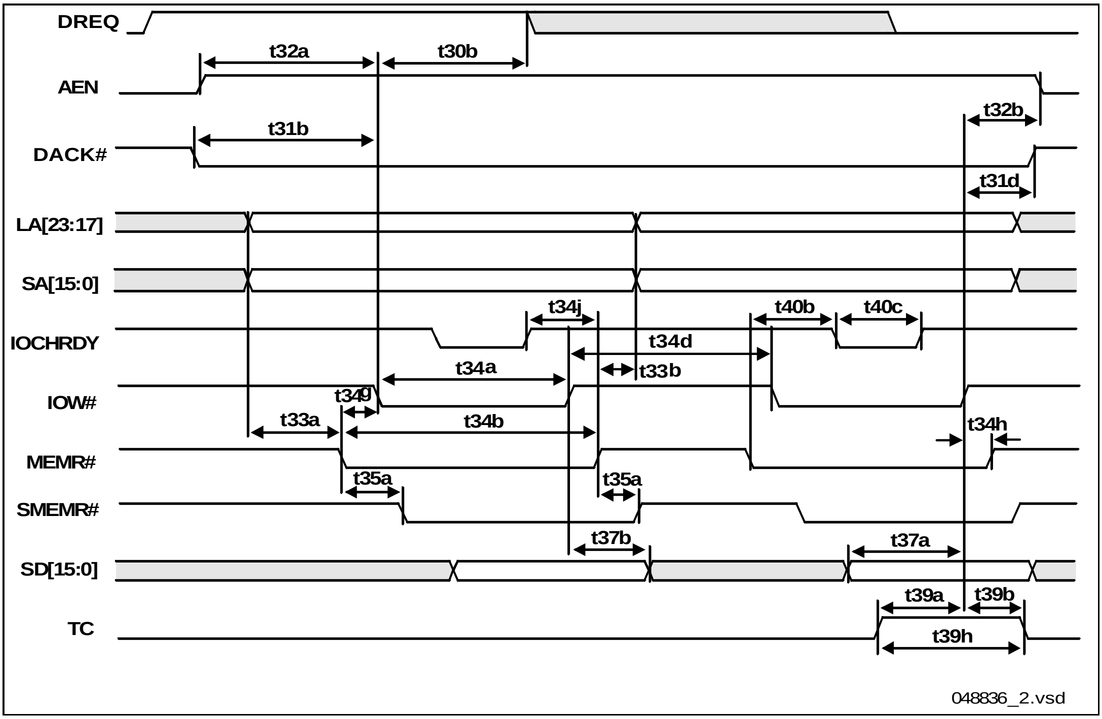

Figure 18. DMA Compatible Timing (Memory Read)

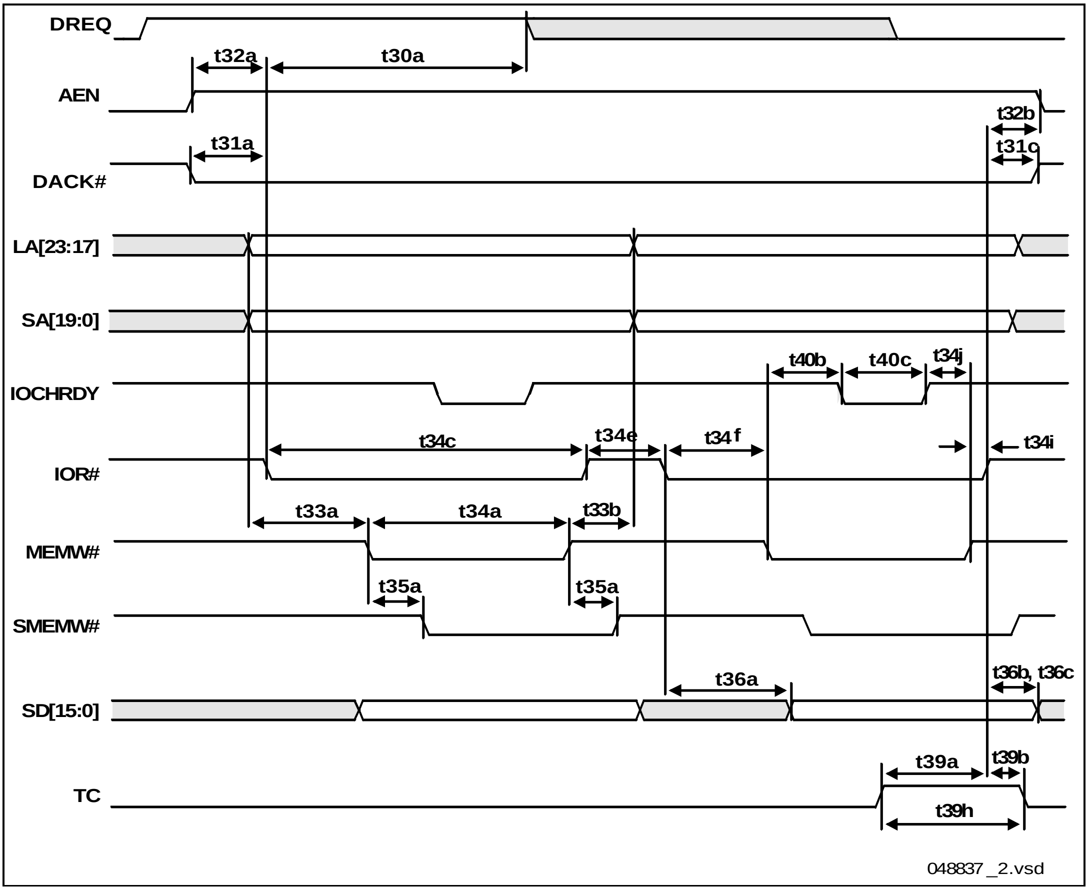

Figure 19. DMA Compatible Timing (Memory Write)

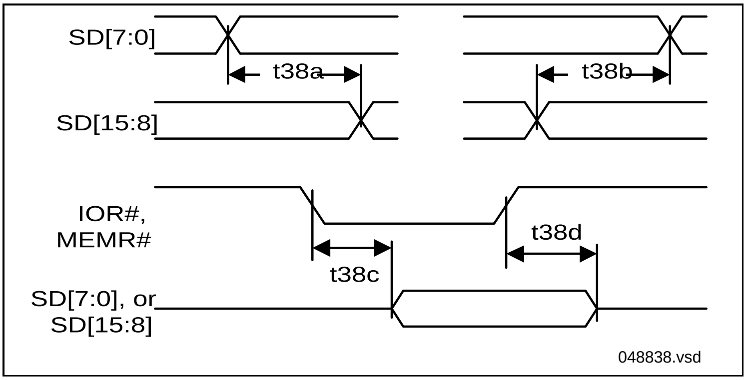

Figure 20. DMA Compatible Timing (Data Swap)

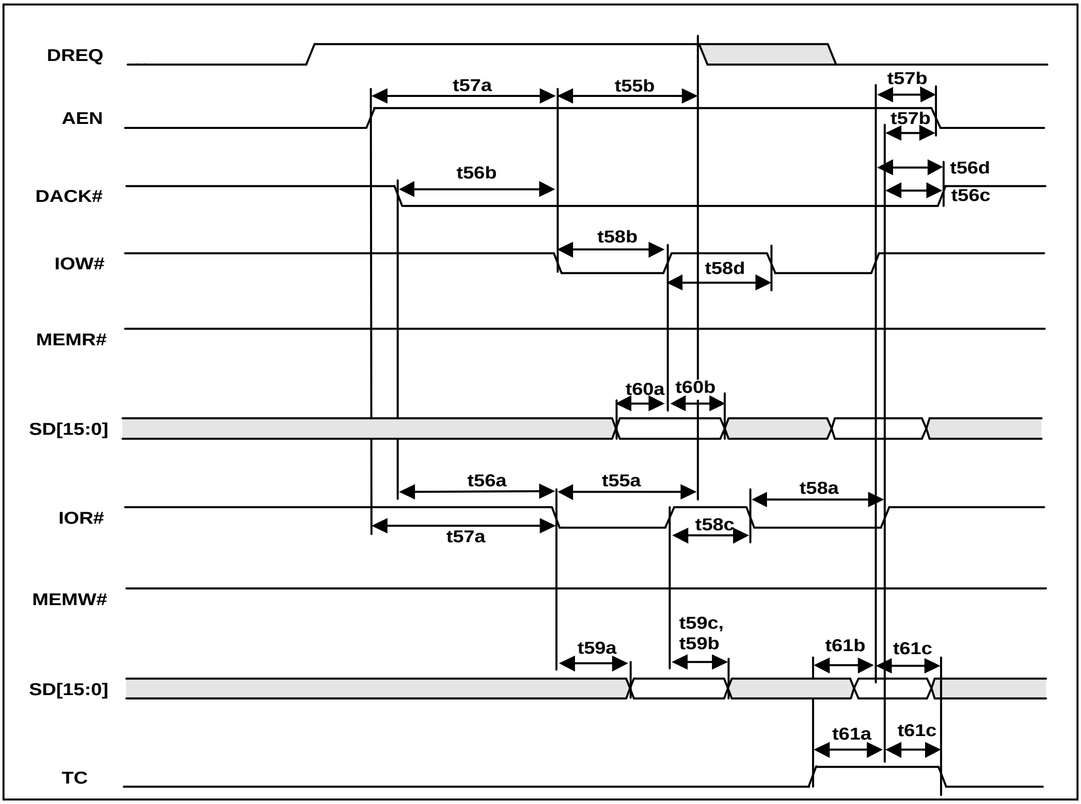

Figure 21. DMA Type F Timing

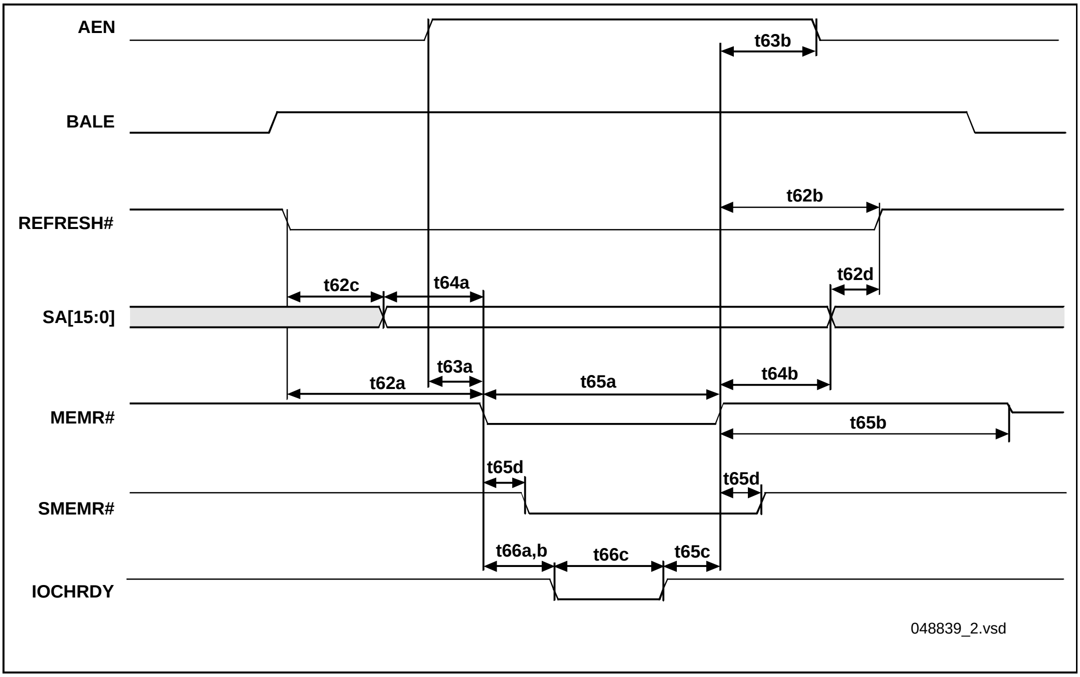

Figure 22. PIIX4-Initiated Refresh Timing

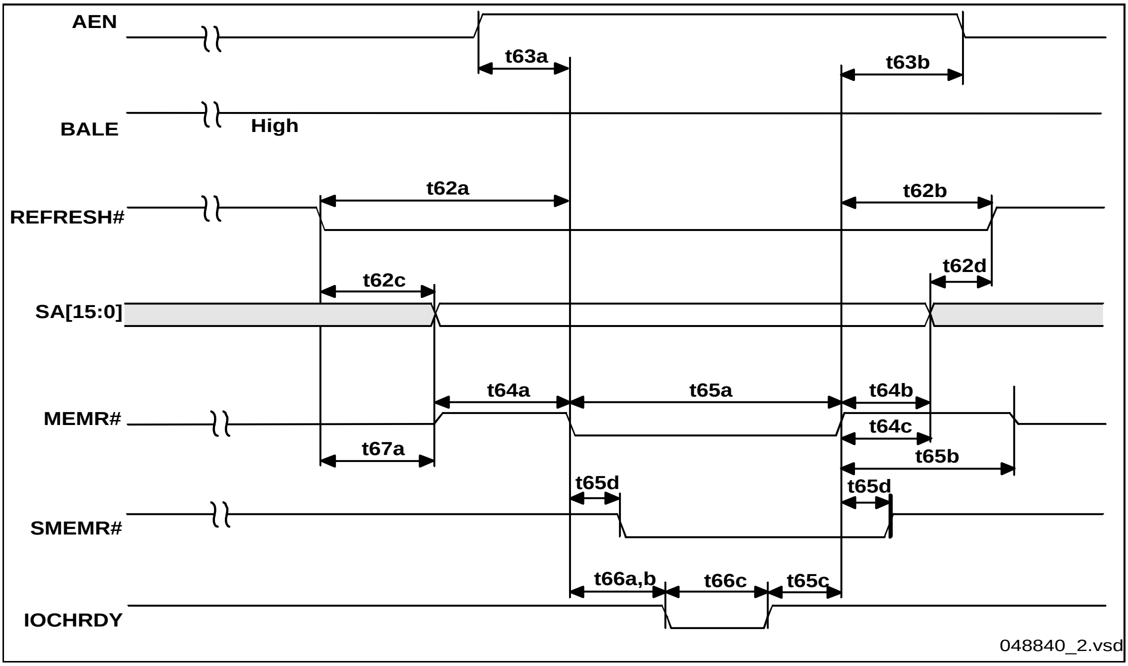

Figure 23. ISA Master-Initiated Refresh Timing

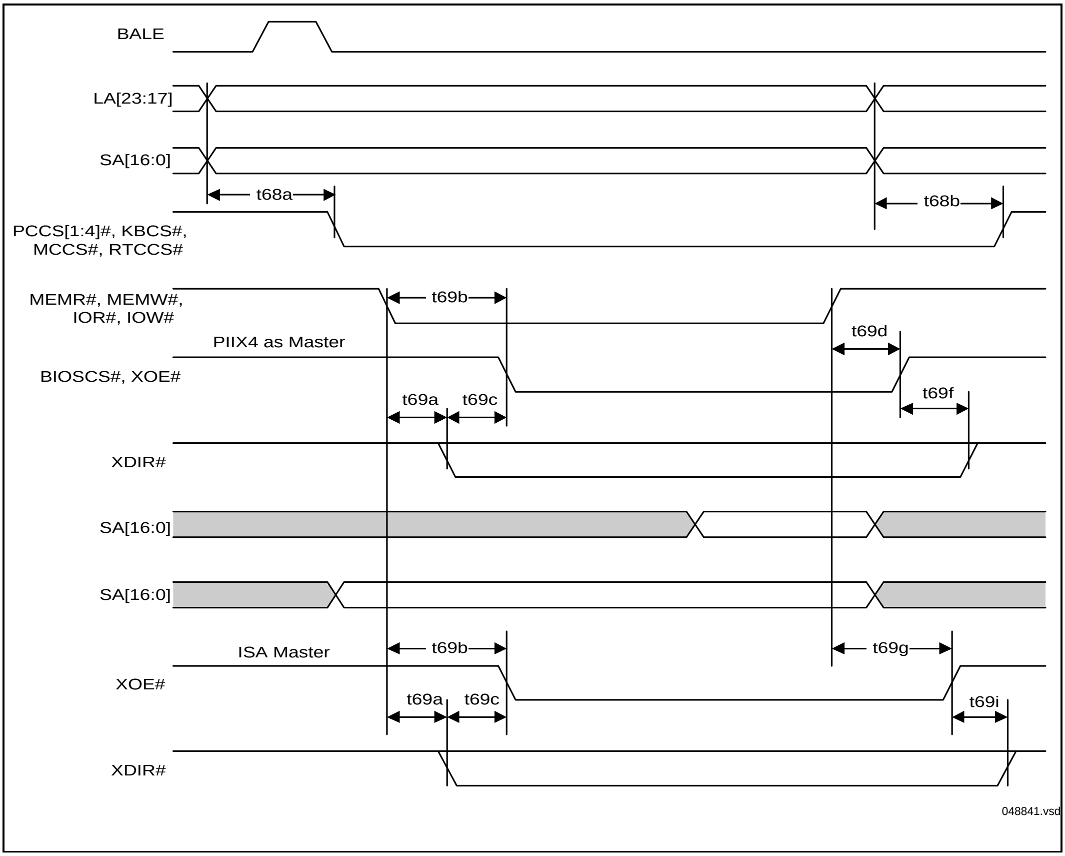

Figure 24. PIIX4 and ISA Master Access to X-Bus Timing

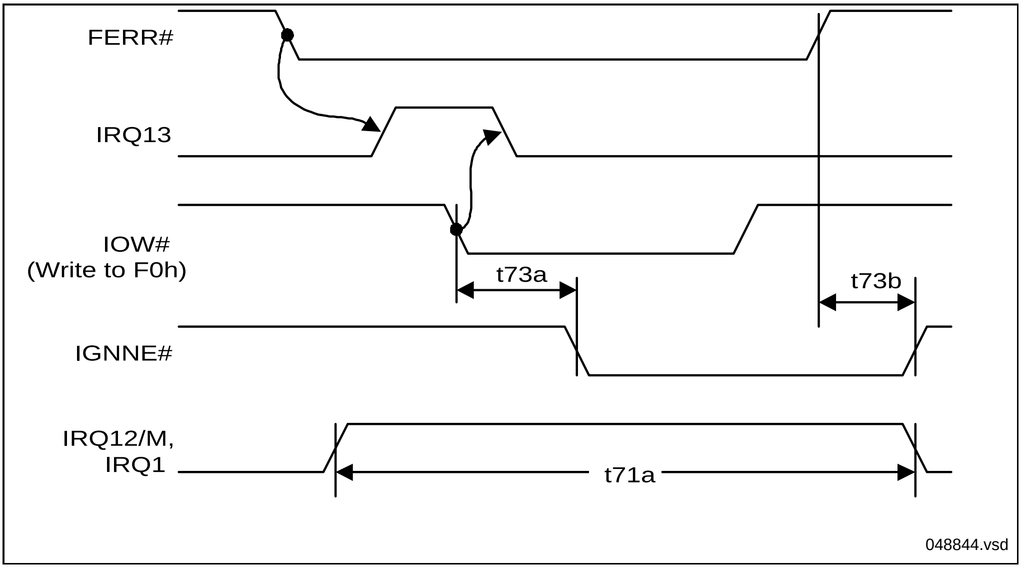

Figure 25. Coprocessor Error and Mouse Support Timing

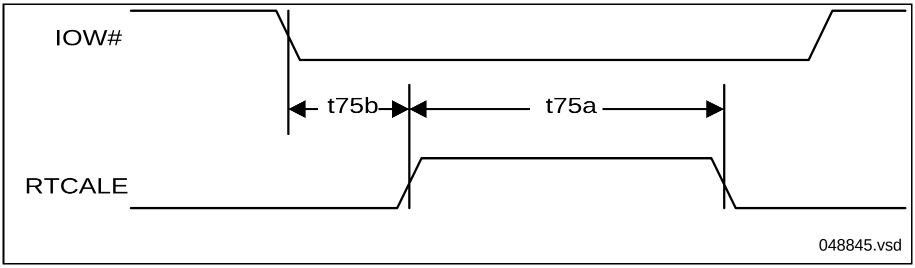

Figure 26. Real Time Clock Timing (RTCALE Generation)

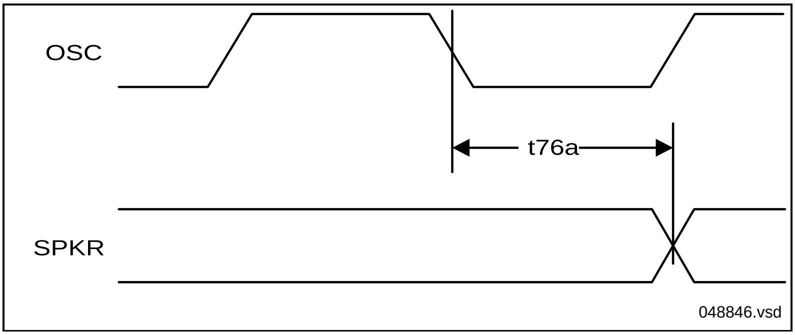

Figure 27. Speaker Timing

2.5 PCI Timing Diagrams

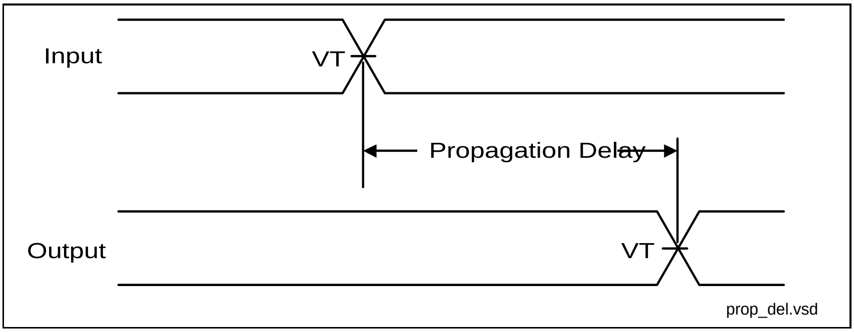

Figure 28. Propagation Delay

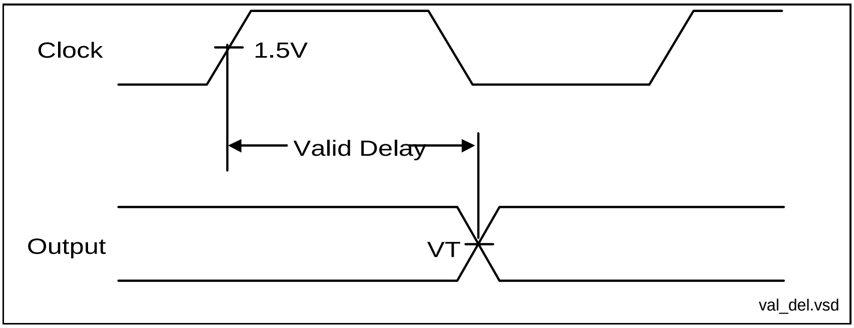

Figure 29. Valid Delay From Rising Clock Edge

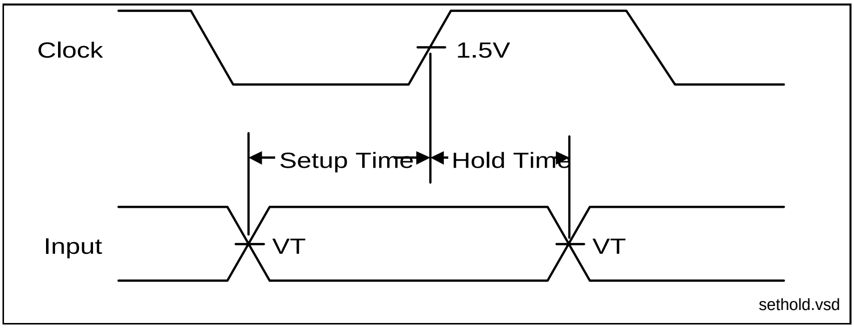

Figure 30. Setup and Hold Times

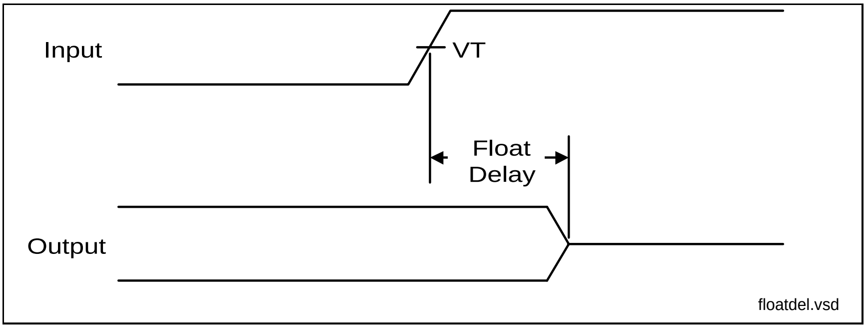

Figure 31. Float Delay

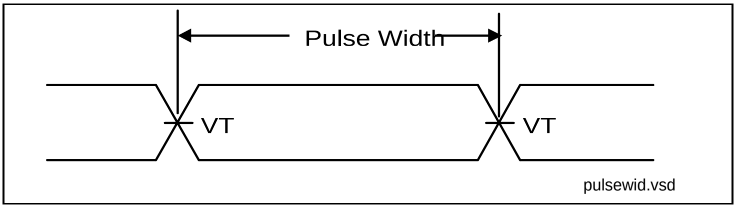

Figure 32. Pulse Width

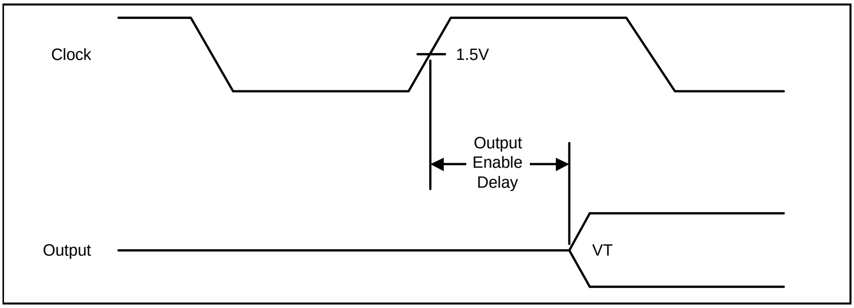

Figure 33. Output Enable Delay

2.6 IDE Timing Diagrams

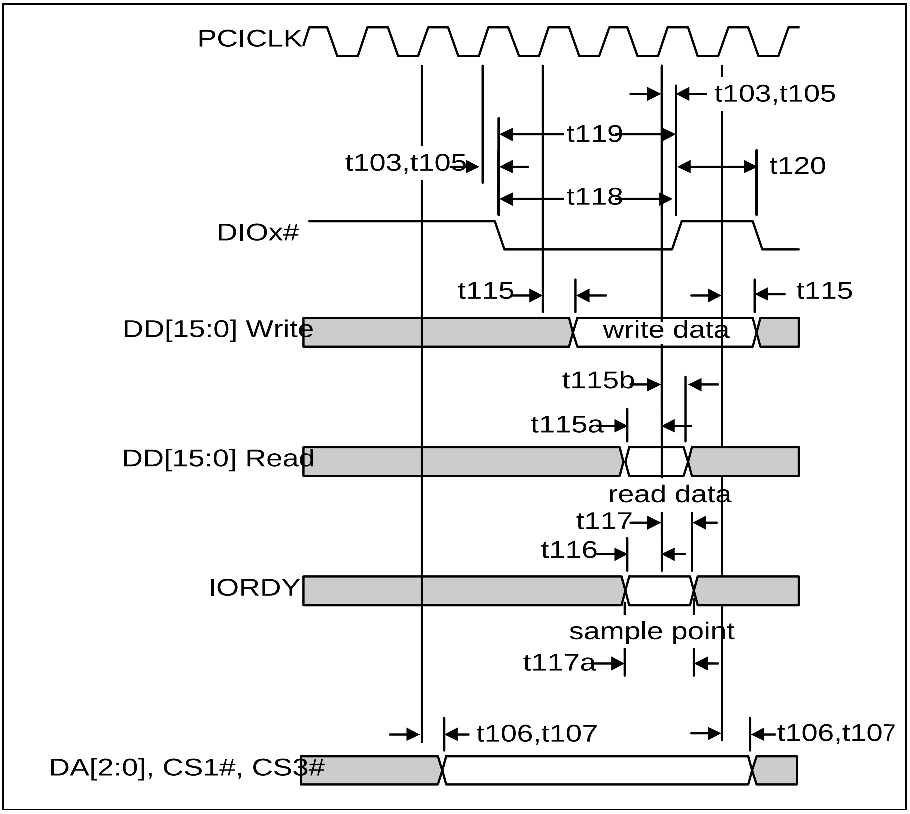

Figure 34. IDE PIO Mode

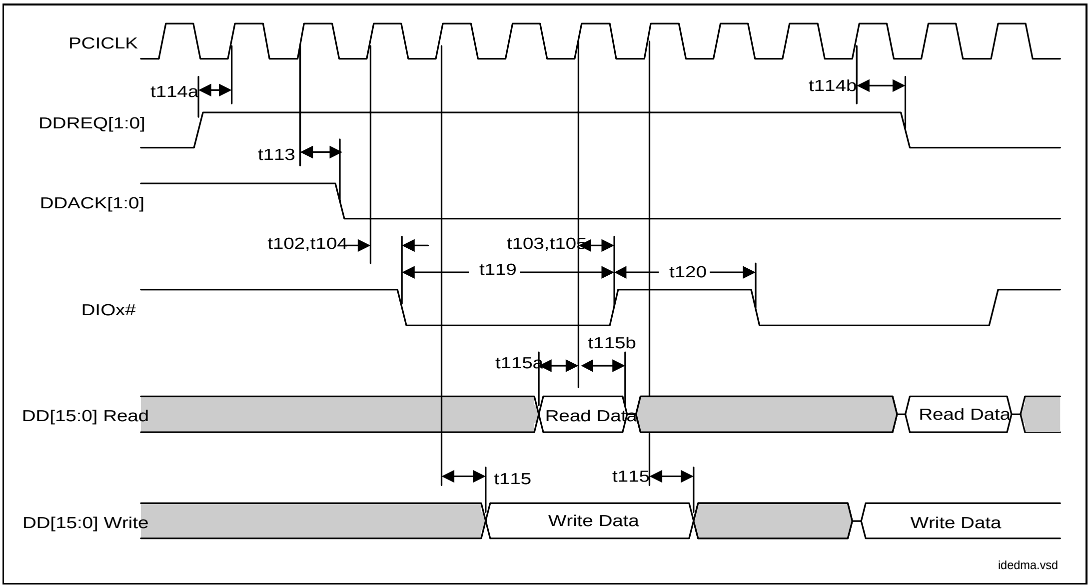

Figure 35. IDE Multiword DMA Mode

2.7 USB Timing Diagrams

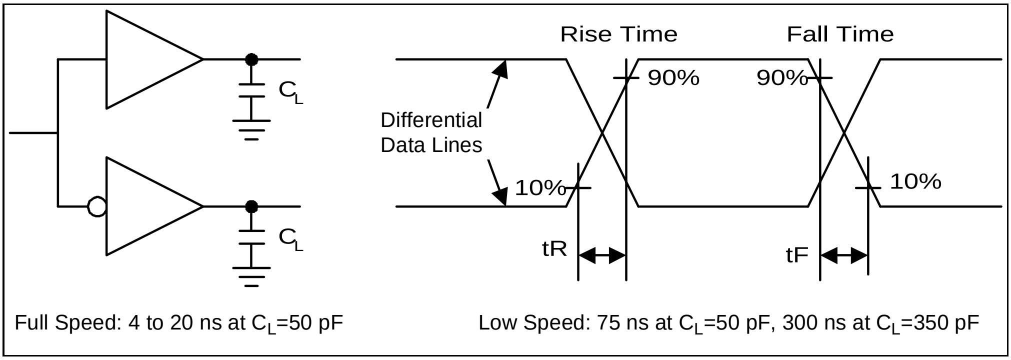

Figure 36. Data Signal Rise and Fall Time

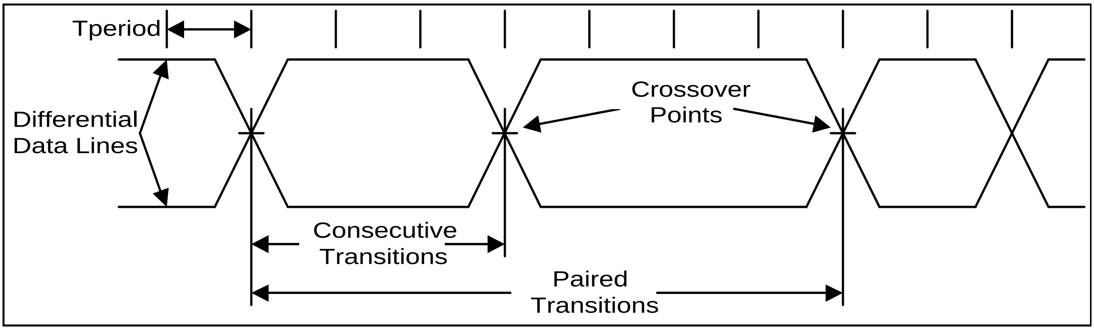

Figure 37. Data Jitter

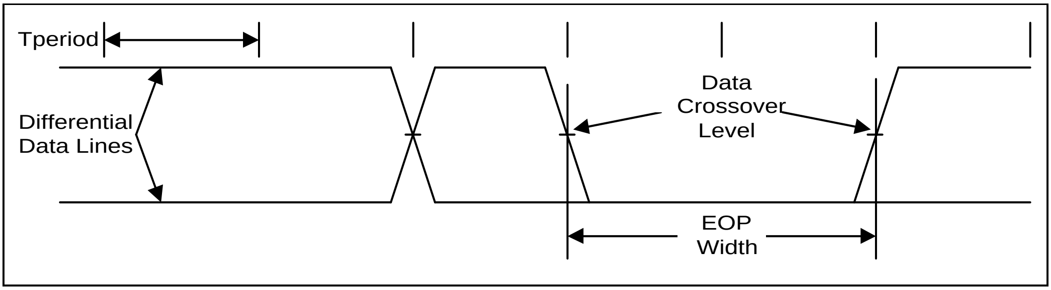

Figure 38. EOP Width Timing

2.8 IOAPIC Timing Diagrams

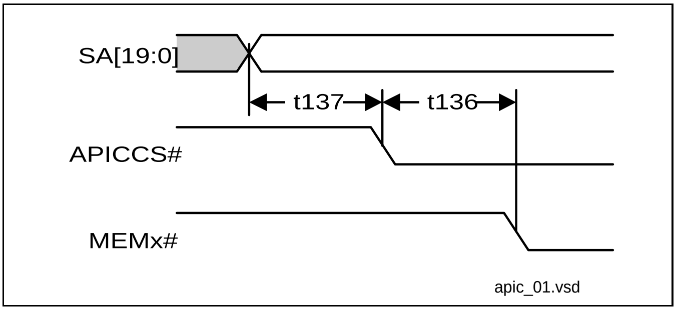

Figure 39. PIIX4 to IOAPIC Timing

2.9 SMBus Timing Diagrams

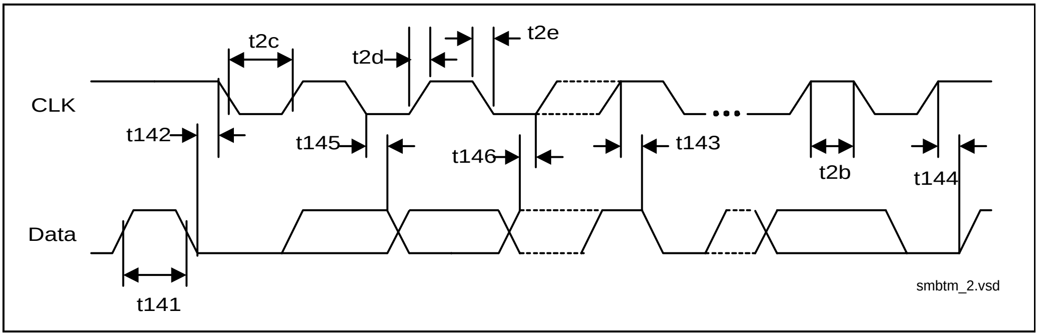

Figure 40. SMBus Timing

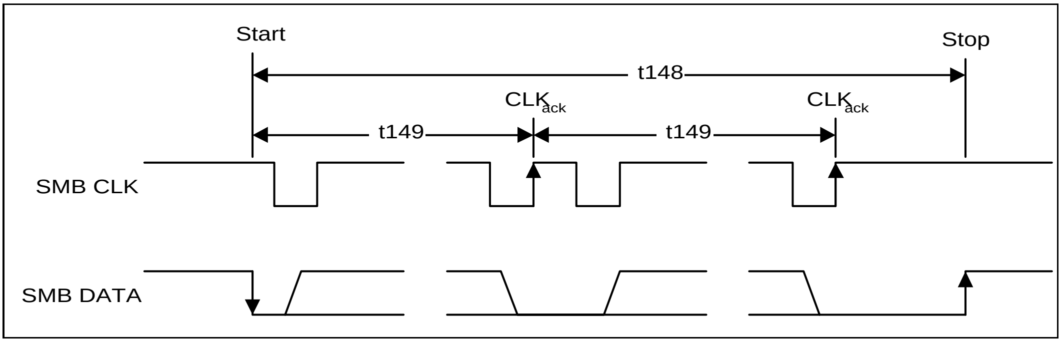

Figure 41. SMBus Timeout timing

2.10 Ultra DMA/33 Timing Diagrams

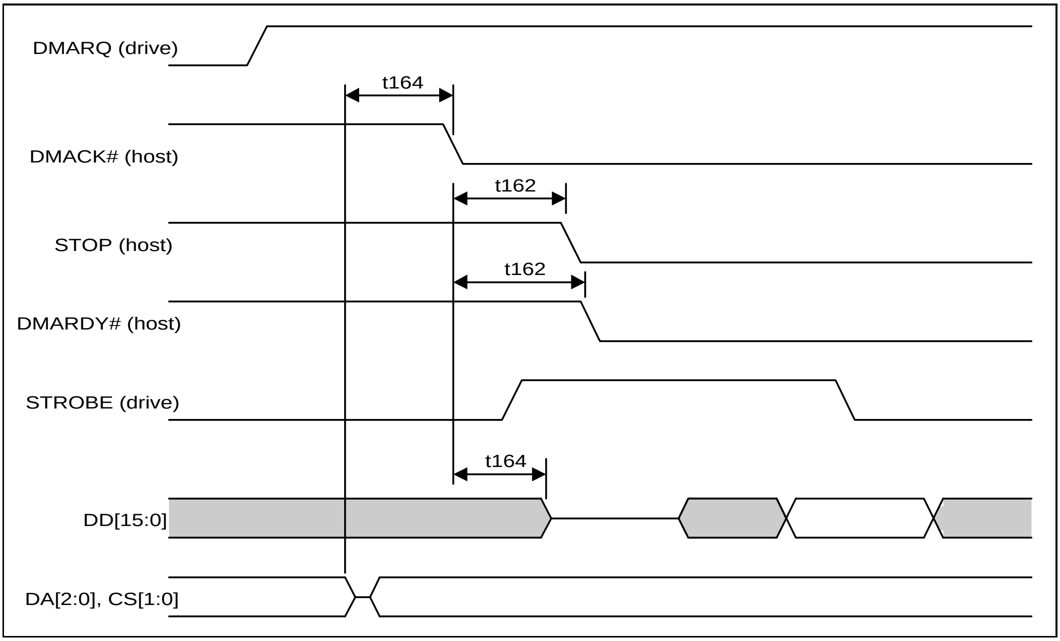

Figure 42. Ultra DMA/33 Drive Initiating a DMA Burst for a Read Command

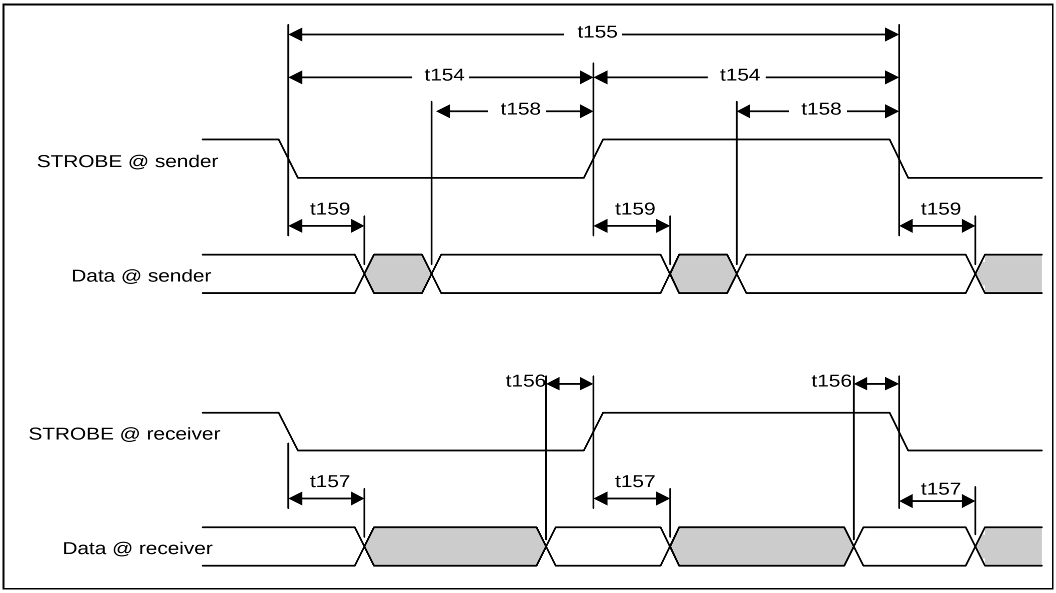

Figure 43. Ultra DMA/33 Sustained Synchronous DMA Burst

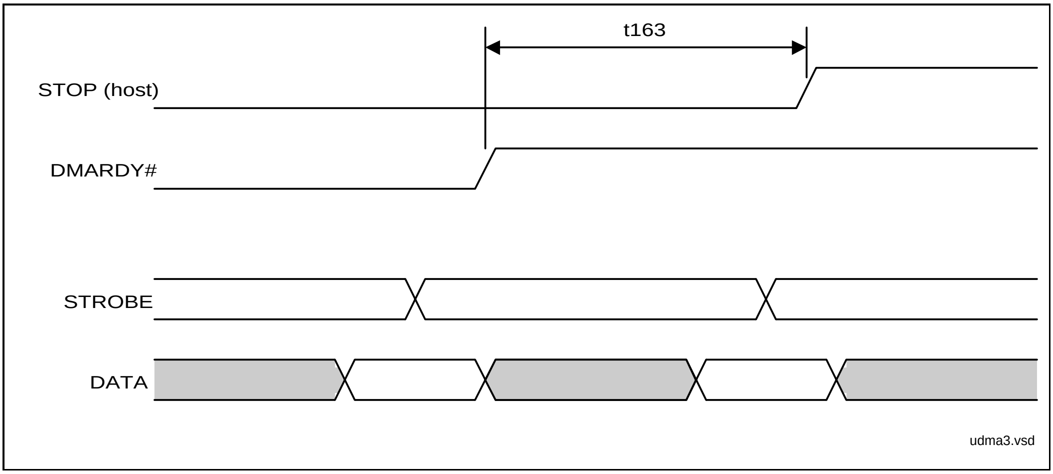

Figure 44. Ultra DMA/33 Sustained Synchronous DMA Burst

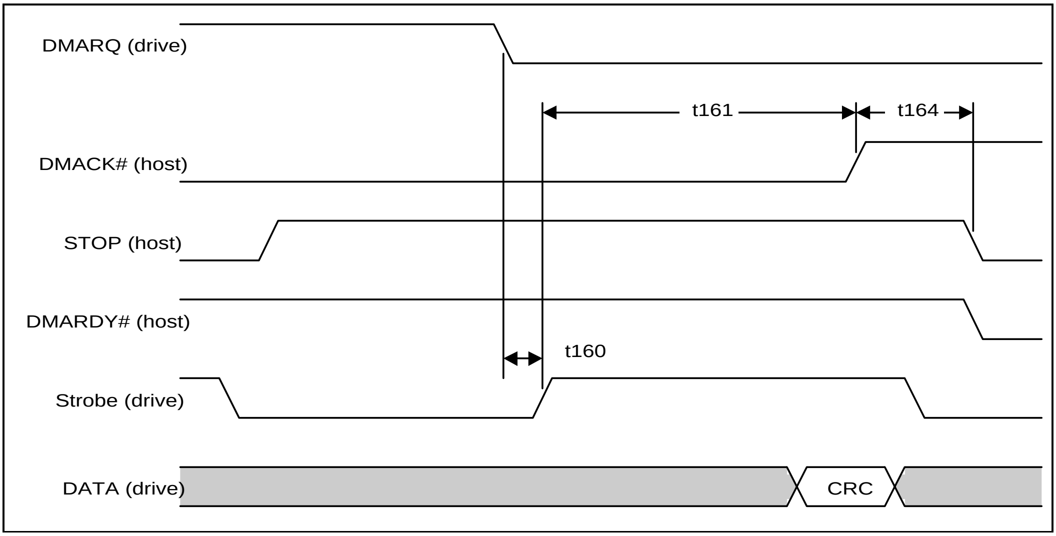

Figure 45. Ultra DMA/33 Host Terminating a DMA Burst During a Write Command